Reliability Comparison of Commercial Planar and Trench 4H-SiC Power MOSFETs

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***Abstract*—The gate oxide reliability, bias temperature instability (BTI), and short-circuit capability for commercial SiC power MOSFETs with planar and trench structures are evaluated and compared in this work. The asymmetric trench MOSFET has the thickest gate oxide among the tested devices, which provides the highest extrapolated gate oxide lifetime from the constant-voltage time-dependent dielectric breakdown (TDDB) measurements. Also, the asymmetric trench structure shows the longest short-circuit withstand time ($SCWT$) benefiting from the adjacent P^+ regions. However, the asymmetric trench MOSFETs show a high threshold voltage shift during the BTI measurements under AC stress, indicating more at or near SiC/SiO_2 interface defects. The double trench MOSFETs also show better short-circuit ruggedness, but no obvious advantages in the TDDB measurements and BTI results.**

***Index Terms*—SiC MOSFET, planar and trench, gate oxide reliability, threshold voltage shift, short-circuit capability.**

I. Introduction

4H-SiC power MOSFETs are being increasingly adopted by automotive companies for their new generation of electric vehicles. The reliability and ruggedness of SiC power MOSFETs attract increasing attention due to the safety-critical nature of the automotive industry. Commercially available SiC power MOSFETs exist in two device structures, the planar double-diffused MOSFET (DMOSFET) and the trench MOSFET (UMOSFET). The conducting channel of the asymmetric trench MOSFET forms along the a-face, and typically has higher electron mobility than the planar MOSFET whose channel forms along the Si-face [1], [2]. Additionally, the trench MOSFET usually has a smaller cell pitch because of the vertically aligned channel. Therefore, a low specific ON-resistance can be realized with trench structure [3]. However, the fabrication process of trench MOSFET is more complex. Oxide electric field also peaks around the bottom corner of the gate trench during device operation. Besides, the different oxidation processes for planar and trench MOSFET result in different gate oxide qualities. Therefore, it is critical to evaluate and compare the reliability of commercially available planar and trench SiC power MOSFETs.

In this work, constant-voltage time-dependent dielectric breakdown (TDDB), AC gate stress bias temperature instability (BTI), and short-circuit measurements are conducted on recently manufactured 650 V and 1200 V commercial SiC planar and trench power MOSFETs. The results are analyzed and compared with respect to the design and processing differences of planar and trench SiC power MOSFETs.

II. Commercial SiC Power MOSFETs

Fig. 1 illustrates the typical cross-sectional views of the tested commercial planar and trench SiC power MOSFETs. The commercial planar power MOSFETs follow the typical double-implanted MOSFET structure (Fig. 1a). The asymmetric trench device has an asymmetric structure (Fig. 1b) where one side of the channel is replaced with a deep P^+ region to better shield the oxide at the bottom corner of the gate trench. For the double trench structure, the source trenches are connected to deep p-wells for the gate oxide electric field shielding and providing body diode conduction. The source trench causes a limitation for the cell pitch. General information of the tested commercial devices is shown in Table I. The gate oxide thicknesses (t_{ox}) is estimated by assuming a dielectric breakdown field of $11\,\mathrm{MV/cm}$ at 150°C [4], [5].

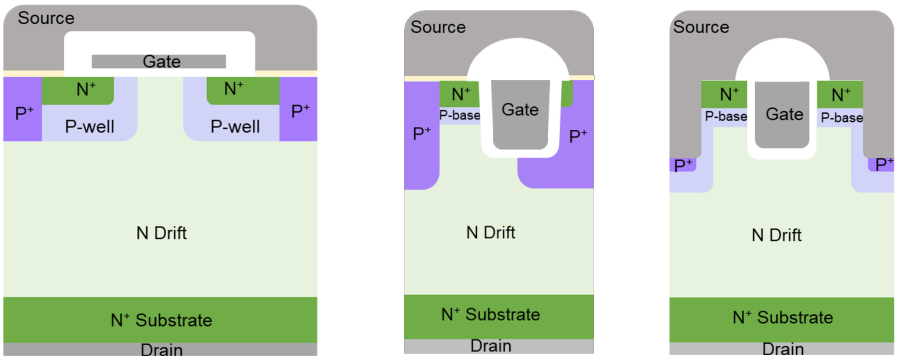
III. Results And Discussion

A. Time-Dependent Dielectric Breakdown (TDDB)

The electron mobility along the vertical trench wall is typically higher than the planar surface. This advantage for

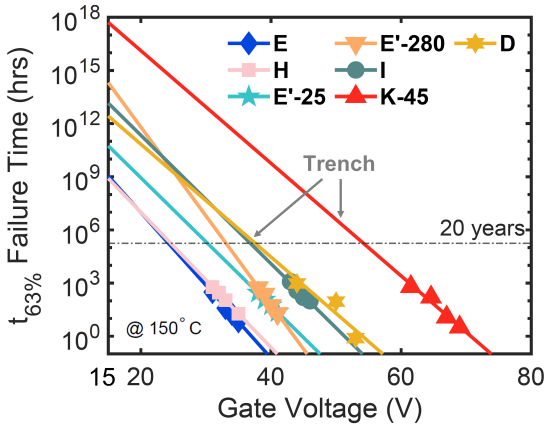
TABLE I: Information for Tested SiC Power MOSFETs.

Vendor	Structure	Estimated t_{ox}	Voltage Rating	Current Rating	ON-resistance
E	Planar	38 nm	1.2 kV	7.6 A	350 mΩ
E'-280	Planar	45 nm	1.2 kV	11 A	280 mΩ
E'-25	Planar	45 nm	1.2 kV	65 A	25 mΩ
C-55	Planar	46 nm	650 V	45 A	55 mΩ
C-550	Planar	46 nm	1.2 kV	12 A	550 mΩ
I	Planar	50 nm	1.2 kV	35 A	75 mΩ
H	Planar	41 nm	1.2 kV	30 A	65 mΩ
K-220	Asymmetric trench	68 nm	1.2 kV	13 A	220 mΩ
K-45	Asymmetric trench	68 nm	1.2 kV	52 A	45 mΩ
D	Double trench	55 nm	1.2 kV	17 A	160 mΩ

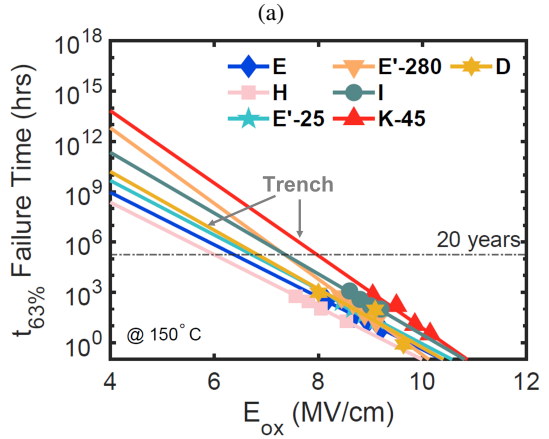


(a) (b) (c)

Fig. 1: Cross-sectional views of (a) planar, (b) asymmetric trench, and (c) double trench SiC power MOSFETs.



(a)



(b)

Fig. 2: 63% failure times vs.(a) gate voltages, and (b) oxide fields for both types of SiC power MOSFETs.

the SiC trench MOSFET is partially traded off for a thicker gate oxide to improve the oxide reliability. As verified in Table I, the commercial trench MOSFETs, especially the asymmetric trench MOSFETs, have thicker gate oxides than the planar devices. Constant-voltage TDDB measurements are conducted for the planar and trench MOSFETs at 150°C. The Weibull distributions are attached in the appendix. The trench MOSFETs show low beta (β) values in the Weibull distribution (Fig. 7f and 7g), indicating larger variations in oxide quality. The extracted 63% gate oxide lifetime ($t_{63}\%$) vs. gate voltages is shown in Fig. 2a. About three orders of magnitude higher gate oxide lifetime are observed on the asymmetric trench MOSFETs at the operational gate voltages (15 V) than all tested planar MOSFETs. The thicker oxide of the asymmetric trench MOSFET directly translates into a significantly higher oxide lifetime. It has also been reported that a thicker oxide allows more effective gate oxide screening thus reducing the failure rate of the products during actual operation [6]. The $t_{63}\%$ vs. oxide field (E_{ox}) is plotted in Fig. 2b. The E_{ox} is calculated using V_G/t_{ox}, where V_G is the corresponding gate voltage in Fig. 2a. The asymmetric trench MOSFET still shows one order of magnitude higher predicted lifetime than the best result from tested planar MOSFETs under the operational gate oxide field ($\sim 4\,\mathrm{MV/cm}$) for planar MOSFETs. The double trench MOSFET has a slightly thicker gate oxide than the tested planar MOSFET. The measured gate lifetime of double trench MOSFET shows minimal advantage compared to planar MOSFET.

The ramped voltage breakdown measurements are conducted on the MOSFETs under 150°C using a Keysight curve tracer B1506A. The results are shown in Fig. 3. Under positive gate bias, the asymmetric trench MOSFET obtains the highest gate oxide breakdown voltage. Both the asymmetric trench and double trench devices can sustain high leakage currents before the oxide breakdown. Leakage current reductions are observed for the trench devices under high positive gate voltages close to the breakdown. This reduction is caused by electron trapping within the oxide as discussed in [4], [7], [8]. Under negative gate bias, the asymmetric trench and double trench MOSFETs also show higher breakdown voltages than the measured planar MOSFETs. Soft oxide breakdown is observed on the double trench MOSFET and planar MOSFET C-550. The same results have been obtained when testing multiple devices from the same vendor. The soft breakdown may be caused by that the damaged spot in the gate oxide happening on the top of the JFET region instead of the N^+ source and channel region [9].

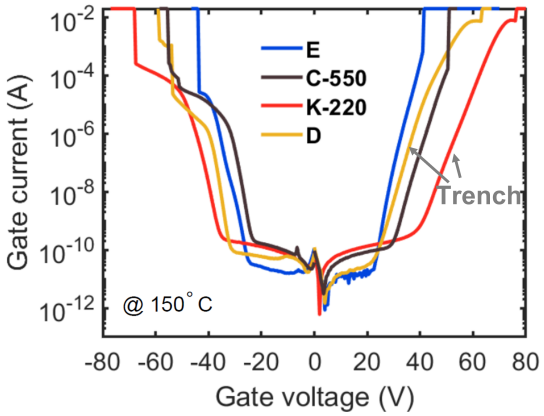


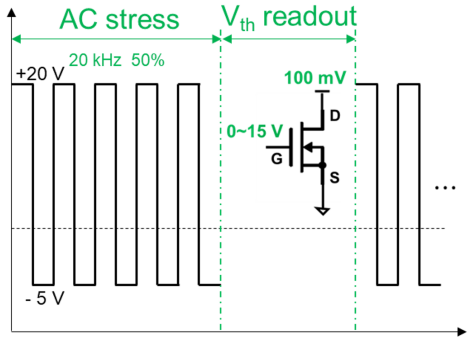
Fig. 3: Positive and negative ramped-voltage breakdown results for both types of SiC power MOSFETs.

B. AC Gate Stress Bias Temperature Instability (AC BTI)

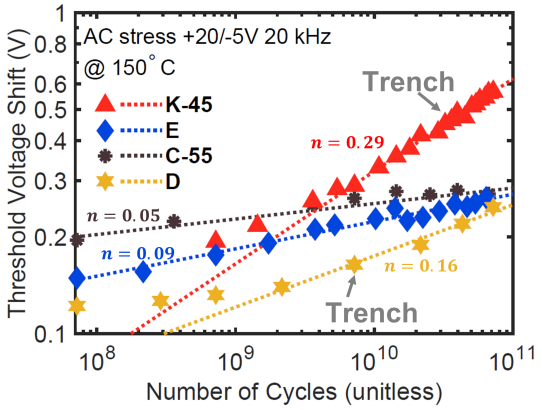
Charge trapping happens at or near the SiC/SiO_2 interface when a gate stress is applied. Device parameters, such as threshold voltage (V_{th}) and ON-resistant (R_{on}), shift due to the trapping phenomenon. The conventional threshold voltage shift (ΔV_{th}) is measured under DC stress conditions known as bias temperature instability (BTI) measurements [10]. To better reflect the device application in a traction inverter, the BTI measurements under AC stress are proposed and used [11]. The AC BTI (+20 V to -5 V) with 20 kHz frequency and 50% duty cycle are applied to the commercial MOSFETs for up to 1000 hours (7.2×10^{10} cycles) at 150°C. The stress is interrupted to read out the V_{th} of the devices. The test sequence is shown in Fig. 4a. The V_{th} is extracted with the linear extrapolation method at 100 mV drain voltage. The average value of the ΔV_{th} vs. the number of cycles is plotted in Fig. 4b and fitted by a power law ($\Delta V_{th} \propto N_{cycles}^{n}$) [11]. The highest V_{th} shift is observed on the asymmetric trench MOSFETs after about 5×10^9 cycles. It has been reported that the V_{th} drift is attributed to the capture and emission of electrons in oxide traps [12]. Therefore, the high V_{th} shift of the asymmetric trench MOSFETs implies a higher density of oxide traps at or near the SiC/SiO_2 interface, which may be introduced by the oxidation process (possibly the deposited oxide). The double trench MOSFETs show the lowest ΔV_{th} among the tested vendors during the 1000-hour measurement. However, the slope of its fitted line is higher than the planar MOSFET results, indicating that the ΔV_{th} of the double trench MOSFETs could exceed the ΔV_{th} of planar MOSFETs if the measurement time is longer than 1000 hours.

C. Short-circuit Withstand Time (SCWT)

Short-circuit (SC) measurements are conducted under a gate bias of 20 V and a bus voltage of 800 V. The drain current waveforms from the last measurement before the device breakdown are recorded. Then, the drain currents are normalized with the corresponding active areas of the devices and shown in Fig. 5. The active areas of the tested devices



(a)



(b)

Fig. 4: (a) Test sequence of the AC BTI measurement. (b) V_{th} shifts for 1000-hour AC BTI tests (each point represents the average ΔV_{th} from ten DUTs. The dash line is the AC fit for each vendor.

are estimated from the bare dies (shown in the appendix), which are obtained by decapsulating the TO-247-3 packages. The active areas and the specific ON-resistance ($R_{on,sp}$) are listed in Table II. Both asymmetric trench and double trench MOSFETs have longer short-circuit withstand time ($SCWT$) compared to the planar MOSFETs (also shown in Fig. 6a). The longer $SCWT$s of the trench MOSFETs may be due to the deep p-type implant regions, which shield the MOS channel from high drain voltage. The two types of trench MOSFETs show similar peak current densities. The asymmetric trench MOSFET has a slightly higher $SCWT$, which may benefit from the asymmetric trench structure that suppresses the drain peak current by the pronounced JFET effect from the adjacent P^+ regions [13]. The structure also allows the current to spread deeper into the device's internal region, away from the top

TABLE II: Estimated active area and $R_{on,sp}$.

Vendor	**Active area** (mm^2)	$\mathbf{R_{on,sp}}$ ($m\Omega \cdot cm^2$)
E	1.16	4.1
C-550	1.91	10.5
K-220	1.36	3.0
D	3.00	4.8

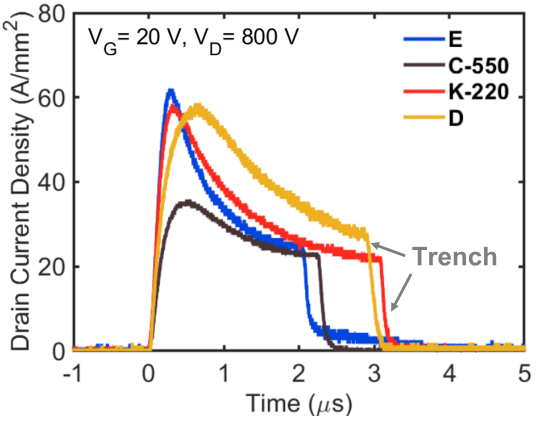


Fig. 5: Drain currents during short circuit events for planar and trench SiC power MOSFETs.

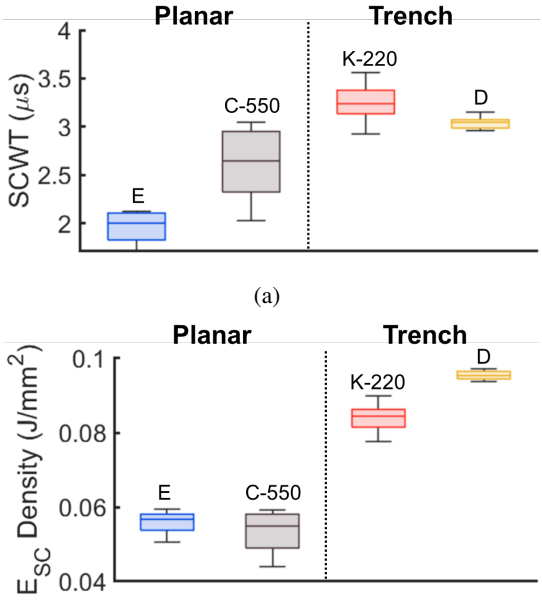


Fig. 6: (a) Short-circuit withstand time ($SCWT$) variations. (b) Energy dissipation during short-circuit event (E_{sc}) variations. (Results from $20 \sim 30$ samples for each vendor).

aluminum metal, and result in a longer $SCWT$.

The energy dissipation during the SC event (E_{sc}) for all the tested samples are normalized and shown in Fig. 6b. Both types of trench MOSFETs show overall higher E_{sc} density than the planar MOSFETs.

IV. Conclusion

TDDB measurements, BTI under AC stress, and short-circuit measurements have been conducted on the planar and trench commercial SiC power MOSFET from different vendors. Benefiting from the thick gate oxide, the commercial SiC asymmetric trench MOSFETs have significantly higher oxide lifetime than the planar MOSFETs under operating conditions as shown by the constant-voltage TDDB. Also, longer $SCWT$s are observed on both types of trench MOSFETs, especially the asymmetric trench MOSFETs, which may be due to the shielding effect from the deep adjacent P^+ regions. A high V_{th} shift for the asymmetric trench is obtained from the AC BTI measurements, indicating more defects at or near the SiC/SiO_2 interface.

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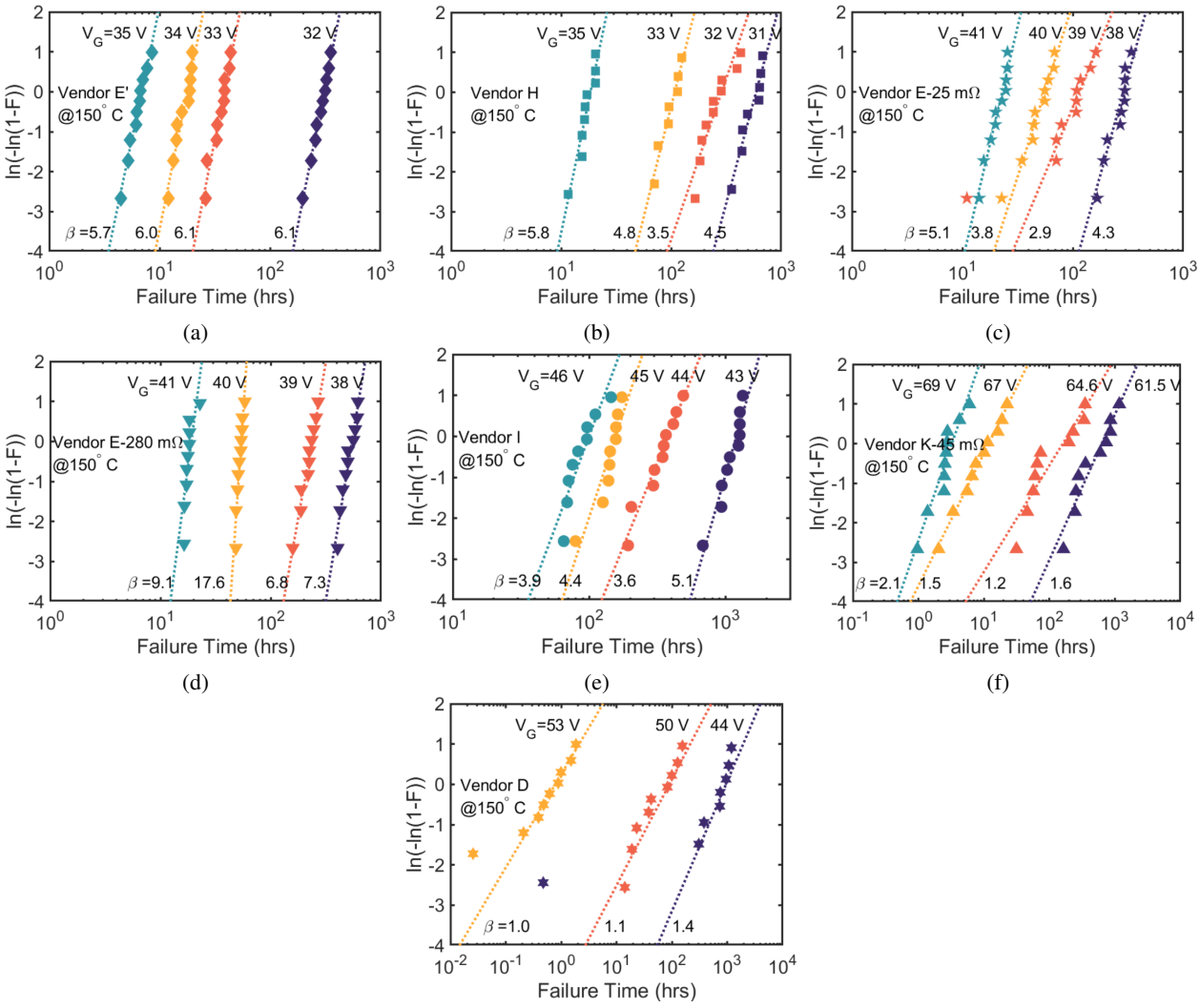
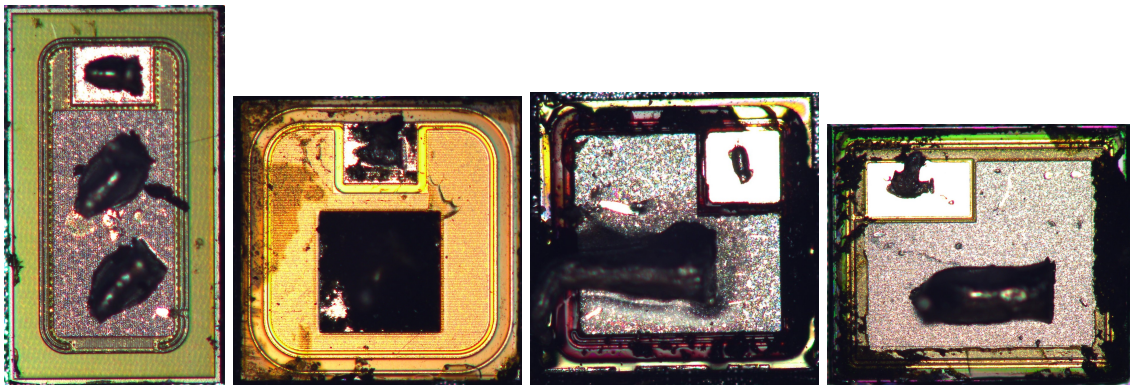
Appendix



(a) (b) (c) (d) (e) (f) (g)

Fig. 7: Weibull distributions for (a)-(e) planar SiC MOSFETs and (f)-(g) trench SiC MOSFETs.



(a) (b) (c) (d)

Fig. 8: Bare dies for tested MOSFET from vendor (a) E, (b) c-550, (c) K-220, and (d) D.