Design of the Drift Layer of 0.6 – 1.7 kV Power Silicon Carbide MOSFETs for Enhanced Short Circuit Withstand Time

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Abstract

We propose a simple technique of raising the short circuit withstand time (SCWT) of 0.6 – 1.7 kV SiC power MOSFETs, where the drift layer resistance is a small fraction of the on-resistance. Using simulations, we show that the SCWT of these devices can be raised by upto 20% by increasing the thickness and lowering the doping of the drift layer at the cost of only 5 % increase in the on-resistance. This approach also raises the breakdown voltage by > 10%. (Keywords: power MOSFET, short circuit withstand time, silicon carbide)

Introduction

SiC Vertical Double diffused power MOSFETs (see Fig. 1) are being used in electric vehicles, traction inverters and charger. During switching, they can experience a Short Circuit (SC) condition, i.e. high voltage between the drain and source terminals simultaneously with a high current, for a small duration. The high power dissipation during this SC condition raises the lattice temperature rapidly, causing thermal runaway or melting of the Al gate contact, thereby creating conducting paths through the oxide and killing the device functionality. The SC duration in which the lattice temperature rises to 1500 K is called the SC Withstand Time (SCWT) [1].

This paper shows how the drift layer of 0.6–1.7 kV devices, where the specific drift layer resistance, R_{dsp}, is a small fraction of the specific on-resistance, R_{onsp}. can be redesigned to increase the SCWT without significantly raising the specific on-resistance, R_{onsp}, or sacrificing the breakdown voltage, V_{BR}.

Design Approach

We derive an approximate formula suitable for qualitative discussion of the dependence of SCWT on structural parameters. Ref. [2] has shown that

$$t_{SC} \approx \frac{C_p\,\rho\,t_d}{V_{DS}\,J_{D,sat}}\Delta T_m, \qquad (1)$$

where C_p, ρ, t_d, V_{DS} and J_{Dsat} are the heat capacity, material density, drift layer thickness, drain to source voltage and drain saturation current density, respectively; ΔT_m is the maximum allowable temperature rise above the ambient before the device is damaged. Large V_{DS} during the SC event causes velocity saturation so that we can approximate $J_{D,sat} \approx qN_d v_{sat}$, where N_d is the doping and v_{sat} is the saturation velocity. The drift layer specific resistance is $R_{dsp} = t_d / qN_d\mu_n$, where μ_n is the mobility. These equations lead to

$$t_{SC} \approx \frac{C_p\,\rho\mu_n}{v_{sat}\,V_{DS}}\Delta T_m R_{dsp}. \qquad (2)$$

This shows that t_{sc} can be raised by increasing R_{dsp}. Numerical simulation is necessary to get realistic values of t_{SC}.

The current design approach minimizes R_{dsp} to minimize R_{onsp}, while yielding the target breakdown voltage, V_{BR}. However, the minimum R_{dsp} is only ~ 15% of R_{onsp} in 0.6 – 1.7 kV devices considered here. Raising R_{dsp} by as much as 35% by lowering N_d and/or raising t_d, raises R_{onsp} by just 5 %. Thus, we can afford to increase R_{dsp} above its minimum value to raise t_{SC}, leading to the following improved design approach.

Lump the components of R_{onsp} other than R_{dsp} into a single resistance, R_{lsp}, so that $R_{onsp} = R_{dsp} + R_{lsp}$, where R_{lsp} is does not vary with N_d or t_d. Let R_{dsp*} and R_{onsp*} represent the minimum values. In the improved design, R_{dsp} is increased to a value which raises R_{onsp} by no more than 5%, i.e. to 1.05 R_{onsp*},

$$R_{dsp} = 0.05R_{onsp*} + R_{dsp*} \qquad (3)$$

Then N_d and t_d are chosen to maximize the V_{BR} for this R_{dsp}. We assume that the maximum V_{BR} point is the same as the maximum $V_{BR,P}$ point, where $V_{BR,P}$ is the breakdown voltage of the plane-parallel base-drift layer junction and has a simpler formula than V_{BR}; V_{BR} ≈ 0.75-0.85 $V_{BR,P}$ due to the curvature effects of the

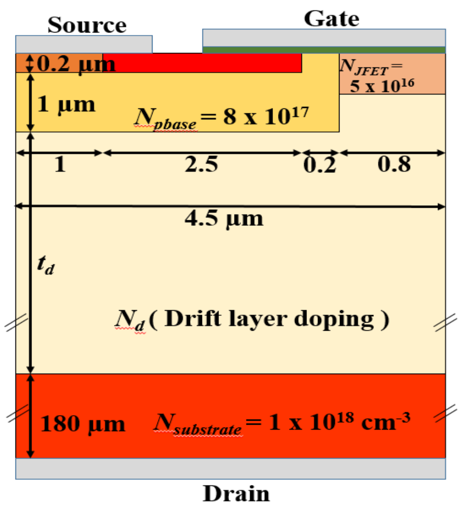


Fig. 1: Device cross-section; the drift layer thickness and doping are varied.

2023 7th IEEE Electron Devices Technology & Manufacturing Conference (EDTM) | 979-8-3503-3252-0/23/$31.00 ©2023 IEEE | DOI: 10.1109/EDTM55494.2023.10103006

Rating (kV)	Ref.	N_d (10^{15} cm^{-3})	t_d (µm)	R_{dsp} (mΩ-cm^2)	R_{onsp} (mΩ-cm^2)	$J_{D,sat}$ (10^4 A cm^{-2})	$V_{BR,P}$ (kV)	t_{SC} (µs)	% increase			
									t_{SC}	V_{BR}	t_d/J_{Dsat}	R_{dnsp}
0.60	[7]	17	5.40	0.23	1.80	3.96	0.96	1.98	13	14	39	35
	OD	15	6.20	0.32	1.89	3.28	1.09	2.24				
1.20	[8]	7.2	11.8	1.16	9.60	2.76	1.92	1.56	20	14	39	38
	OD	6.0	13.7	1.64	10.1	2.30	2.19	1.87				
1.70	[9]	5.7	14.5	1.80	10.3	2.44	2.30	1.50	19	11	33	28
	OD	4.9	16.4	2.32	10.8	2.04	2.55	1.78				

Table 1 Existing designs reported in literature compared with our design (OD). R_{dsp} for existing design is calculated from (3) and (8)-(11) while that for our design from (5). R_{onsp}, J_{Dsat}, $V_{BR,P}$, t_{SC} are simulated values. R_{onsp} of OD is 1.05 times that of existing design.

edge termination. At breakdown, the field in the drift layer of the plane-parallel base-drift layer junction falls linearly from the critical field, E_C [3], so that

$$V_{BR,P} = E_C t - \frac{1}{2\epsilon_s} q N_d t^2 \tag{4}$$

Substituting for t_d in terms of N_d from $R_{dsp} = t_d / qN_d\mu_n$, we get

$$V_{BR,P} \approx qN_d \mu_n E_C R_{dsp} - \frac{1}{2\epsilon_s} q^3 N_d^3 R_{dsp}^2 \mu_n^2 \tag{5}$$

Treating R_{dsp} as constant, ignoring the dependence of E_C and μ_n on N_d, and then setting $dV_{BR,P}/dN_d = 0$. we solve for N_d as

$$N_d = \sqrt{\frac{2\epsilon_s E_C}{3q^2 \mu_n f R_{dsp}}}, \tag{6}$$

whose substitution into R_{dsp} yields

$$t_d = \frac{2\epsilon_s E_C}{3qN_d}, \tag{7}$$

We solve for N_d iteratively from (6) and the following equation [3]-[4], where N_d is in cm^{-3}, and get t_d from (7)

$$E_c = 2.56 \times 10^4 \; N_d^{1/8} \text{ V cm}^{-1}, \tag{8}$$

$$\mu_n = 40 + \frac{950-40}{1+\left(\frac{N_d}{2\times10^{17}}\right)^{0.76}} \text{ cm}^2\,\text{V}^{-1}\text{s}^{-1} \tag{9}$$

We now demonstrate the improvement in SCWT due to new design approach using numerical simulations.

Simulation Setup and Calibration

Electro-thermal simulations were performed using ATLAS simulator. Fig. 1 shows the device structure. The drift layer parameters - N_d and t_d are varied as per Table 1. Our simulations show that the addition of an edge termination such as floating field rings does not affect SCWT. We include the temperature and surface scattering effects on mobility by employing the Canali model for bulk and Lombardi CVT model for channel mobilities. Temperature dependence on thermal conductivity and heat capacity are included too. Bottom contact is treated as a thermode with a thermal resistance. Model parameters are calibrated against measurements of [5] in the following sequence. Mobility parameters are calibrated using I_D-V_{GS} and I_D-V_{DS} curves. Next, the heat capacity and thermal conductivity parameters are calibrated using I_D versus time data. The simulations so calibrated gave a SCWT of 10 µs which is within 5% of the measured value. We also simulated $V_{BR,P}$ using the Selberherr's impact ionization model with parameters calibrated as in [6].

Results and discussions

Fig. 2 compares the simulated drain current and temperature transients during the SC event for existing and our improved designs for a 0.6 kV device. The details of the two designs appear in Table I, where the 0.6 – 1.7 kV voltage rating in column 1 is

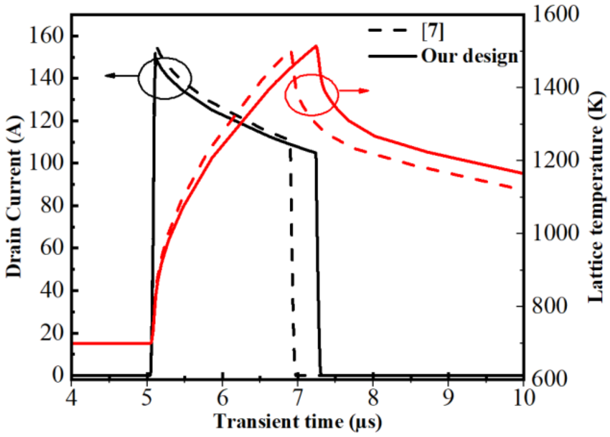
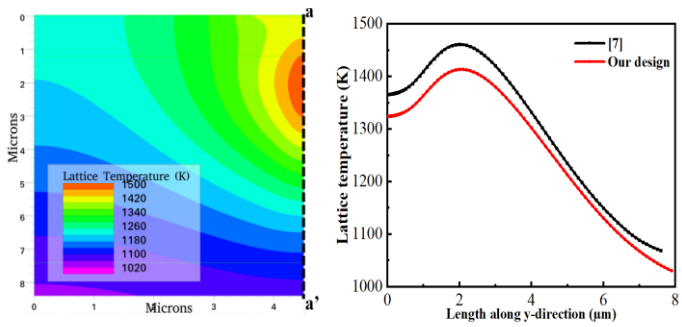


Fig. 2 Transient simulations of the drain current and temperature rise during the short circuit event for the 0.6 kV device having the structure of Fig. 1, drift layer doping and thickness given in Table I, and V_{DS} = 480 V, V_{GS} = 20 V.



(a) (b)

Fig. 3 (a) Temperature distribution at the end of the short circuit event for the 0.6 kV device having the structure of Fig. 1, drift layer doping and thickness of [7] given in Table I, $V_{DS} = 480$ V and $V_{GS} = 20$ V. (b) Temperature variation from gate to drain contact along the cut-line a-a' shown in (a) for the device from [7] and our design.

the device blocking voltage demanded by the application. The V_{BR} is higher to provide safety margin, and $V_{BR,P}$ is even higher to compensate for the curvature effects of the edge termination junctions. Fig. 3(a) gives the spatial distribution of the temperature within the device to reveal the location of the peak temperature point below the JFET region. Fig. 3(b) shows that the peak temperature in our design is 40 K lower. Table I summarizes the existing and improved designs of various devices from state-of-the-art academic and industrial facilities, and the simulated R_{onsp}, $J_{D,sat}$, SCWT and $V_{BR,P}$ for these. These results are better understood with the help of Table I. Our design is seen to increase SCWT by 13-20 % and $V_{BR,P}$ V_{BR} by 11-14 % at the cost of only 5 % higher R_{onsp}. Table I allows us to ascertain the validity of (1) and of the approximation (2) employed to derive (4). As per (1), the SCWT should increase by the same factor as the ratio $t_d/J_{D,sat}$. However, is seen that only 33-57 % of the increase in $t_d/J_{D,sat}$ translates to the increase in SCWT, implying that (1) needs major improvement to be able to replace numerical simulation. On the other hand, the last two columns of the table show that the % increase in R_{dsp} is 0.84-1.06 times that of $t_d/J_{D,sat}$. This implies that (2) is as good as (1) and the approximation (2) is valid.

Conclusion

We showed that the short circuit withstand time of 0.6 – 1.7 kV devices can be raised by upto 20% by increasing the thickness and lowering the doping of the drift layer at the cost of only 5 % increase in the on resistance. This approach also raises the breakdown voltage by > 10%.

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