Effects of Oxide Electric Field Stress on the Gate Oxide Reliability of Commercial SiC Power MOSFETs

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***Abstract*— In this work, the influence of various oxide electric field (E_{ox}) stress conditions on the gate oxide lifetime, gate leakage current, and threshold voltage of 1.2 kV 4H-SiC power planar metal-oxide-semiconductor field-effect transistors (MOSFETs) is investigated. The results suggest that high E_{ox} stress (> 9.4 MV/cm) applied to the gate oxide of commercial SiC power MOSFETs for a certain period degrades the oxide lifetime due to high Fowler-Nordheim (F-N) electron tunneling current followed by hole trapping. Moreover, hole trapping enhances the gate leakage current and reduces the threshold voltage. Therefore, the generation of holes under high electric field conditions should be avoided to ensure the reliability of SiC power MOSFETs.**

Keywords*— Gate oxide reliability, electron and hole trapping, lifetime, gate oxide electric field stress, threshold voltage shift, leakage current

I. Introduction

SiC power devices are predominantly utilized in power supplies and electric vehicles, so the gate oxide reliability of SiC power MOSFETs influences the operational lifetime of these industrial applications. There are various issues that affect the reliability of gate oxide, such as higher defect density in the oxide limiting the lifetime [1], SiC/ SiO_2 interface traps resulting in charge trapping and a threshold voltage shift [2]. Compared with Si, SiC MOS structures have more early gate oxide failures. Therefore, an efficient screening method is required to screen out a significant number of extrinsic failures without degrading the intrinsic lifetime of the gate oxide. High gate voltage screening is a fast and effective method to screen out extrinsic defects [3], but impact ionization and/or anode hole injection (AHI) can be triggered under higher gate voltages which produce hole trapping in the gate oxide. The trapped holes increase the gate leakage current and decrease the threshold voltage of SiC power MOSFETs [4]. It has been shown that higher gate tunneling currents lead to reduced intrinsic gate oxide lifetimes [5]. Additionally, a negative shift of the threshold voltage can lead to increase in the OFF-state drain-leakage current. Therefore, it is valuable to find suitable oxide electric field stress and stress time that can satisfy application requirements without severely decreasing V_{th} and reducing gate oxide lifetime.

This work focuses on the effect of different oxide electric field stresses and stress times on the reliability of the gate oxide layer. The time-dependent dielectric breakdown (TDDB) results for commercial SiC power MOSFETs with and without stress are compared and discussed in terms of gate oxide lifetime prediction after being exposed to a variety of gate voltage stress conditions. The gate leakage currents and threshold voltage shifts of SiC power MOSFETs under high and low E_{ox} conditions are also monitored to investigate the gate oxide reliability.

II. Device and Experimental Methods

A. Devices

The commercial 1.2 kV 4H-SiC planar power MOSFETs (packaged in TO-247) from vendor E are tested in this work. Table 1 contains the general characteristics of commercial 1.2 kV SiC planar MOSFETs. Fig. 1 depicts the cross-sectional view of a typical planar power MOSFET. A semiconductor parameter analyzer (B1506A, Keysight, Inc) is used to test the relevant parameters of SiC MOSFETs. The threshold voltages are extracted at V_{DS} = 0.1 V using the linear extrapolation approach [6]. The on-resistances are obtained with V_{DS} = 1 V and the maximum allowable gate voltage. When measuring gate oxide breakdown voltages (V_{BR}) at 150°C, the source and drain terminals of the devices under test (DUTs) are shorted to the ground while the gate voltage is ramped up and the gate leakage current is measured until dielectric breakdown. The oxide thicknesses are estimated based on the average oxide breakdown voltages at 150°C, with the assumption that the critical oxide breakdown electric field is 11 MV/cm (t_{ox} = V_{ox}/E_{ox}). The gate oxide breakdown voltage for vendor E is extracted to be ~ 49.46 V at 150°C. Thus, the oxide thickness is ~ 45 nm.

TABLE I. Tested Commercial 1.2kV SiC Planar Mosfets

Properties	Vendor E
Mean V_{th} @RT (V)	5.94
Typical R_{on} @RT (mΩ)	280
Mean oxide V_{BR} @150°C (V)	49.46
Estimated t_{ox} (nm)	45

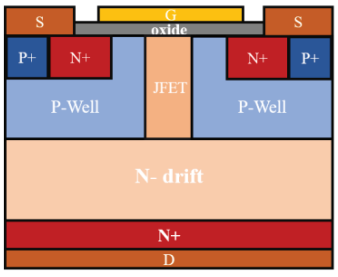

Fig. 1. A typical cross-sectional view of a commercial SiC planar power MOSFET.

B. EXPERIMENTAL METHODS

Constant-voltage TDDB measurements are performed on commercial 1.2 kV 4H-SiC power planar MOSFETs to obtain the gate oxide lifetime at 150°C. Ten devices as a group are carefully selected to make sure the threshold voltage variation among each group is less than 0.1 V. A constant gate voltage

is applied to all 10 DUTs' gate electrodes at the same time, with their source and drain electrodes grounded. Failure times are recorded using a 10-channel digital multimeter (DMM 6500, Keithley, Inc), and the data is analyzed using Weibull statistics (method described in more details in [7, 8]). The Weibull distribution is obtained from the TDDB results to extract the 63% gate oxide lifetime ($t_{63\%}$) under different E_{ox} conditions. The oxide lifetime under typical operating conditions can be predicted based on the widely known thermo-chemical E-model [9].

To investigate the effects of different voltage stresses on the reliability of commercial SiC MOSFETs respectively, various gate oxide stress conditions are separately applied to commercial SiC power MOSFETs. After the stress, the following constant-voltage TDDB measurements are performed at 150°C with different gate voltages. The effect of gate stress conditions on the gate oxide reliability of SiC MOSFETs is investigated by comparing the changes in gate oxide lifetime before and after stress.

The threshold voltages and leakage currents have been recorded under different gate oxide voltages. The B1506A semiconductor parameter analyzer is utilized to provide the gate voltage and measure the curves of leakage current and threshold voltage over time to determine the influence of E_{ox} stress. Before the test and after every stress period, the threshold voltage at 150°C is extracted, as shown in Fig. 2. The gate leakage current is recorded during the stress period.

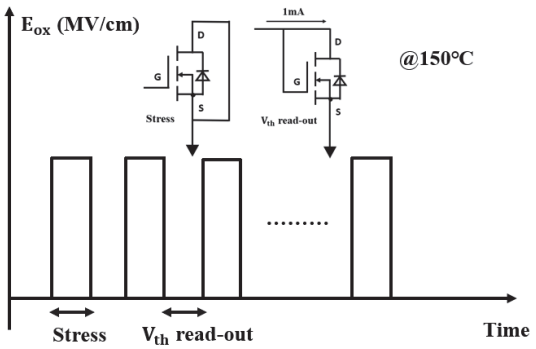

Fig. 2. Test procedure for gate leakage current and threshold voltage at 150°C

III. Experimental Results

A. TDDB measurements on un-stressed commercial SiC MOSFETs

The trend of gate leakage current vs. time varies depending on the electric fields of the gate oxide layer. Fig. 3 shows gate leakage current under different gate oxide electric fields of SiC MOSFETs from Vendor E. The applied E_{ox} varies from 8.5 MV/cm to 9.9 MV/cm. When the E_{ox} is less than 9 MV/cm, the gate leakage current of the DUTs decreases until the oxide layer breaks down. However, when the E_{ox} is higher than 9 MV/cm, the gate leakage current of the device rises initially then decreases until breakdown.

In our previous research, the variation of gate leakage current under different gate voltage conditions can be explained by hole trapping and electron trapping [10]. For the SiC MOSFETs from Vendor E, hole trapping originating from impact ionization and/or AHI dominates under high E_{ox} conditions, which reduces barrier width. As a result, electron injection and trapping of electrons in the gate oxide increase. However, when electron trapping dominates, the gate leakage current decrease due to the increase in barrier width. Therefore, under high E_{ox} (> 9 MV/cm) conditions, a large number of electrons and holes get trapped in the oxide. At a low E_{ox} (< 9 MV/cm), it is mainly electrons that are captured by traps both near the interface and in the oxide layer.

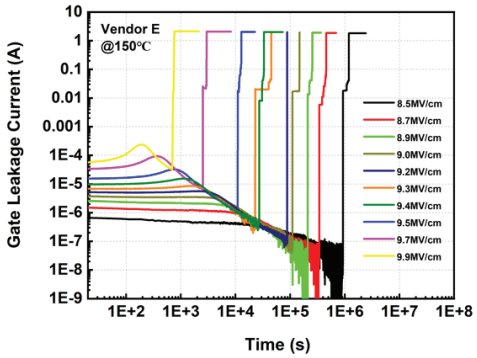

Fig. 3. Gate leakage current under different E_{ox} of SiC MOSFETs from Vendor E.

A group of gate oxide electric fields is chosen for the TDDB measurements: 8.5 MV/cm, 8.7 MV/cm, 8.9 MV/cm, 9.2 MV/cm, 9.5 MV/cm, 9.7 MV/cm, and 9.9 MV/cm. Ten devices with similar V_{th} are measured at each E_{ox}. Based on the Weibull plot, the failure time ($t_{63\%}$) for each E_{ox} is extracted and displayed in Fig. 4. Two different field acceleration factors (slopes of the fitted lines) are detected. An abrupt change in field acceleration factors is observed at E_{ox} of ~ 9.4 MV/cm. This is because when the E_{ox} exceeds 9.4 MV/cm, the hole trapping effect becomes more pronounced, causing higher F-N tunneling current thus degrading the gate oxide lifetime. Fig. 4 illustrates the extracted $t_{63\%}$ as a function of E_{ox} for commercial SiC MOSFETs from Vendor E. According to the thermo-chemical E-model, the predicted oxide lifetime at E_{ox} of 4 MV/cm and 150°C is above 3×10^{10} hours.

The transition from where electron trapping dominates to where hole trapping dominates happens at E_{ox} = 9 MV/cm. Gate oxide screening techniques are commonly used in the industry to remove extrinsic failures. If hole trapping dominates, the F-N tunneling current would increase and accelerate the degradation of the gate oxide. Therefore, in the subsequent tests, the effect of different E_{ox} stress on the gate oxide lifetime of commercial SiC MOSFETs is investigated.

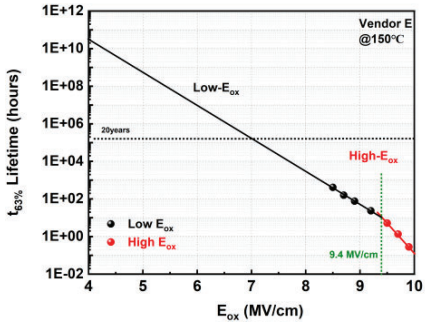

Fig. 4. The extracted $t_{63\%}$ as a function of E_{ox} for commercial SiC MOSFETs

B. TDDB measurements on commercial SiC MOSFETs after E_{ox} stress

In the previous study, it has been observed that high E_{ox} can induce a dominant effect of hole trapping and then reduce the lifetime of the gate oxide layer. Therefore, 1min @ 9.7 MV/cm, 1min @ 9.9 MV/cm, and 100 ms @ 9.9 MV/cm are chosen as the electric field stress conditions to investigate the impact of high voltage stress on the gate oxide lifetime.

In Fig. 5, the oxide lifetimes of SiC MOSFETs with and without E_{ox} stress at 150°C are compared. The lifetimes of some of the MOSFETs after stress are higher than the MOSFETs without any stress. This may be caused by the variation of the oxide lifetime due to fabrication process variation for different MOSFETs. Due to the limitation on the number of samples, no significant lifetime degradation is observed for devices exposed to 1 min at 9.7 MV/cm and 100 ms at 9.9 MV/cm stress. It is observed that the Weibull slop (β) reduces after 1 min 9.9 MV/cm stress, reflecting considerable variations in the oxide failure time. The reduction in β demonstrates the adverse effect of high E_{ox} stress on the gate oxide reliability.

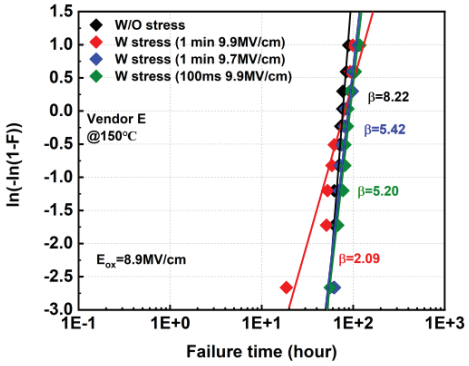

Fig. 5. Weibull distributions of measured lifetimes at 150°C for commercial SiC MOSFETs with stress and without stress.

To make the effect of stress more pronounced, initial electric field stress of 9.9 MV/cm is applied to the gate and maintained for three minutes at 150°C, and then the gate electric field is reduced to lower E_{ox} (8.5MV/cm, 8.7MV/cm, and 8.9MV/cm) for the TDDB test in order to extract the gate oxide lifetimes. The measured lifetimes for SiC MOSFETs with 3 min at 9.9 MV/cm stress and without stress are plotted in Fig. 6 (a). The intrinsic lifetime of the original device is 15 min at E_{ox} of 9.9 MV/cm and 150°C as shown in Fig. 4. When the applied stress time is 20% of the oxide lifetime at E_{ox} of 9.9 MV/cm, the oxide lifetimes of the device after the stress at low E_{ox} are reduced to ~10% of the original oxide lifetime. As shown in Fig. 6 (a), the predicted lifetime at 4 MV/cm for SiC MOSFETs without stress is ~ 10^{10} hours. However, SiC MOSFETs with 3 min 9.9 MV/cm stress have approximately two orders of magnitude reduction in lifetime prediction at 4 MV/cm.

A low E_{ox} stress condition of 8 MV/cm for 10 hours is used as a comparison. Fig. 6 (b) illustrates $t_{63\%}$ vs E_{ox} at 150°C for commercial SiC MOSFETs with 10 hours at 8 MV/cm stress and without stress. The measured oxide lifetimes indicate that a prolonged stress at a low electric field does not significantly degrade the gate oxide lifetime.

It is believed that high E_{ox} stress (> 9.4 MV/cm) has a harmful impact on the lifetime of oxide, while low electric field stress has less obvious influence on the lifetime of gate oxide since there is no enhanced F-N tunneling current caused by hole trapping.

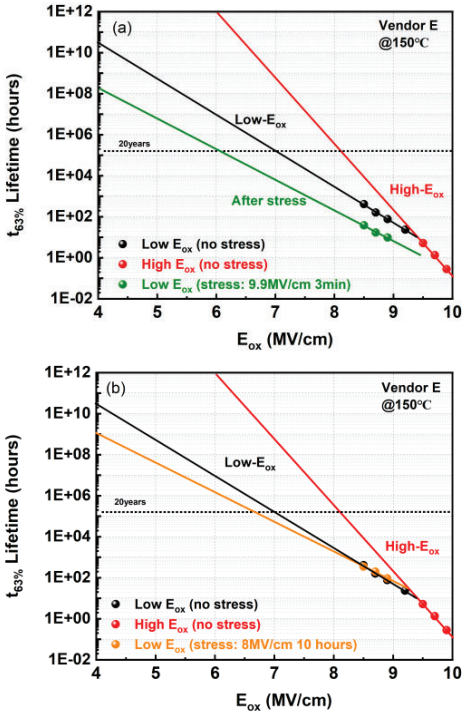

Fig. 6. $t_{63\%}$ vs E_{ox} at 150°C for commercial SiC MOSFETs with (a) 3 min 9.9 MV/cm stress and (b) 10 h 8 MV/cm stress.

C. Gate leakage currents and threshold voltage shifts

Under different E_{ox} conditions, the positive and negative charge trapping near the interface and inside the oxide layer affects the value of the threshold voltage, whereas the variation of the leakage current reveals the electron and hole distribution inside the oxide. The mechanisms of hole and electron trapping under varied oxide electric fields are discussed to explain the different gate leakage trends and related threshold voltage variations.

The threshold voltages and leakage currents under different E_{ox} conditions have been recorded at 150°C, as depicted in Fig. 7. When E_{ox} = 8 MV/cm, leakage current gradually decreases with time. So it can be assumed that electron trapping plays a dominant role under the electric field of 8 MV/cm. With the increase of stress time, a large number of electrons gradually get trapped in the oxide layer, and these electrons enhance the barrier width and shift threshold voltage in a positive direction. When E_{ox} = 8.9 MV/cm, similar trends can be observed for leakage current and threshold voltage. The threshold voltage shift values are 0.27 V and 0.13 V for 8 MV/cm and 8.9 MV/cm electric field stress conditions, respectively, when the stress time is 0.1 s. Hole generation diminishes part of the effect of electron trapping at E_{ox} of 8.9 MV/cm, so that a smaller threshold voltage shift value can be obtained when 8.9 MV/cm is applied for 0.1 s. After 1000 s of E_{ox} stress, more electrons are trapped in the gate oxide at 8.9 MV/cm, and the threshold voltage shift value is 1.84 V.

During the 9.9 MV/cm stress period, the barrier width decreases due to the prominent function of hole trapping, resulting in an increased leakage current over a period of 140

s, while the threshold voltage decreases with time, as shown in Fig. 7. However, after 140 s of stress at 9.9 MV/cm, electron trapping is the primary effect, leading to a drop in leakage current and an increase in threshold voltage.

A higher screening voltage improves the screening efficiency and reduce the field-failure probability after screening. While the high gate voltage comes with the challenge of negative threshold voltage shift. Fig. 8 illustrates the threshold voltage shift after applying 100 ms E_{ox} stress to the gate oxide at 150°C. It can be observed that the threshold voltage shows a negative shift when E_{ox} is greater than 9 MV/cm. To avoid the negative threshold voltage shift, it is recommended to use a E_{ox} less than 9 MV/cm as the electric field for gate oxide screening.

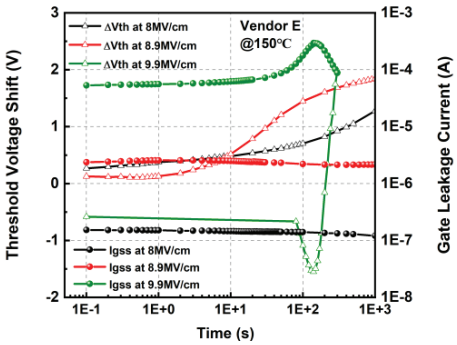

Fig. 7. Threshold voltage variations and gate leakage currents during gate voltage stresses at various E_{ox} for SiC MOSFETs from Vendor E.

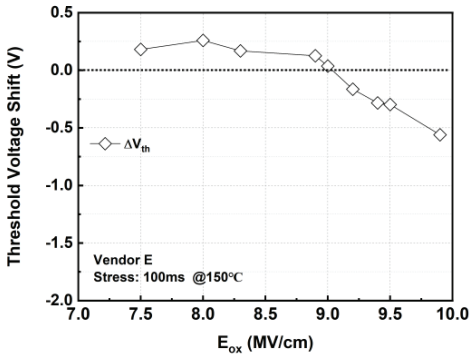

Fig. 8. Threshold voltage shift at various E_{ox} for SiC MOSFETs from Vendor E.

IV. Conclusion

The changes in gate oxide lifetime, leakage current, and threshold voltage after different E_{ox} stresses are shown in this paper. When E_{ox} is greater than 9.4 MV/cm, a large F-N tunneling current is generated due to hole trapping, thus degrading gate oxide lifetime. In addition, a negative threshold voltage shift is observed at E_{ox} value higher than 9 MV/cm. The transition from where electron trapping dominates to where hole trapping dominates happens at oxide electric field of 9 MV/cm. To avoid a reduction in threshold voltage and prevent degradation of gate oxide lifetime, the screening E_{ox} should be below 9 MV/cm.

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