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SPICE Modeling and CMOS Circuit Development of a SiC Power IC Technology

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***Abstract*—This paper presents the SPICE modeling and circuit development of a SiC power integrated circuit (IC) technology that offers monolithic integration of high-voltage lateral n-type SiC power metal-oxide-semiconductor field-effect transistors (MOSFETs) and low-voltage SiC complementary-MOS (CMOS) devices. The SPICE models are based on two-dimensional device simulations with the Sentaurus TCAD device simulator. With the developed SPICE models, this technology enables the design of application specific integrated circuits (ASICs) in SiC, such as fully integrated high-voltage SiC power converters, that can work in high temperature and radioactive environments. Circuit simulations of a SiC CMOS inverter and a SiC ring oscillator are included to demonstrate the technology.**

***Index Terms*—SiC ICs, CMOS design in SiC, Power ICs, SPICE modeling.**

I. Introduction

Currently, the main focus of the silicon carbide (SiC) technology is on discrete power devices, such as SiC vertical power MOSFETs, because the larger bandgap and higher breakdown electric field of SiC allow superior SiC-based power electronics compared to their silicon (Si) counterparts [1], [2]. These inherent material properties also make SiC integrated circuits (ICs) attractive in specific applications, such as subterranean and interplanetary explorations and high-temperature data acquisition [3], where the electronics operate under harsh environments. Therefore, SiC ICs have also gained attention.

SiC IC research began in the 1990s, where the early studies were conducted on both 6H-SiC and 4H-SiC wafers with low-voltage (LV) all n-type MOSFET (NMOS) processes [4]–[6]. With material and process improvement, Raytheon Systems Limited (RSL) developed a 1.2-μm 4H-SiC complementary metal–oxide–semiconductor (CMOS) process (HiTSiC). A process design kit (PDK) was also developed for this process [7]. Since then, various LV SiC CMOS circuits have been demonstrated with the HiTSiC process and its PDK [3], [8]–[13]. Recently, Barlow et al. reported a SiC CMOS gate driver that can drive CREE 3rd generation SiC power MOSFETs at over 500°C [3].

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SiC bipolar junction transistors (BJTs) and SiC junction field-effect-transistors (JFETs) based ICs have also been developed for extreme-temperature operations. Hou et al. reported a 16x16 SiC BJT-based UV image sensor array operational at 400°C [14]. Neudeck et al. [15] have also demonstrated SiC JFET-based digital ICs that operate across a wide range of temperature span (−190°C to 812°C).

Previous SiC IC efforts focused on low-voltage applications. This work presents a SiC power IC technology that offers monolithic integration of high-voltage (HV) lateral SiC power MOSFETs and low voltage SiC CMOS devices. The proposed technology enables application specific integrated circuits (ASICs) in SiC, such as fully integrated SiC power converters to operate at elevated temperatures with higher power ratings. Level 2 SPICE models are developed based on two-dimensional (2-D) TCAD simulations for both the LV CMOS and HV NMOS devices. Simulations of a SiC CMOS inverter and a SiC ring-oscillator are demonstrated with the developed SPICE models.

II. 2-D TCAD Simulation

Fig. 1 shows the cross-sectional views of the SiC HV NMOS, LV NMOS, and LV PMOS. All MOSFETs are designed with the Sentaurus TCAD device simulator, and the simulations are based on an actual fabrication process in collaboration with the team at the ADI Hillview facility. The N-type drift layer is 6 μm thick and with $2.5 \times 10^{16} cm^{-3}$ doping concentration. The

TABLE I
TCAD Simulations for SPICE Parameter Extractions

I-V simulaitons	Simulation conditions	SPICE parameters
Ids vs. Vgs	Vds=0.1 V Vgs=0∼25 V, step=50 mV Vbs=0∼-6 V, step=-1 V	VTO, GAMMA, NSUB, PHI, UO, UEXP, UCRIT
Ids vs. Vds	Vbs=0 V Vds=0∼25 V, step=0.5 V Vgs=0∼25 V, step=5 V	LAMBDA, VMAX, NEFF

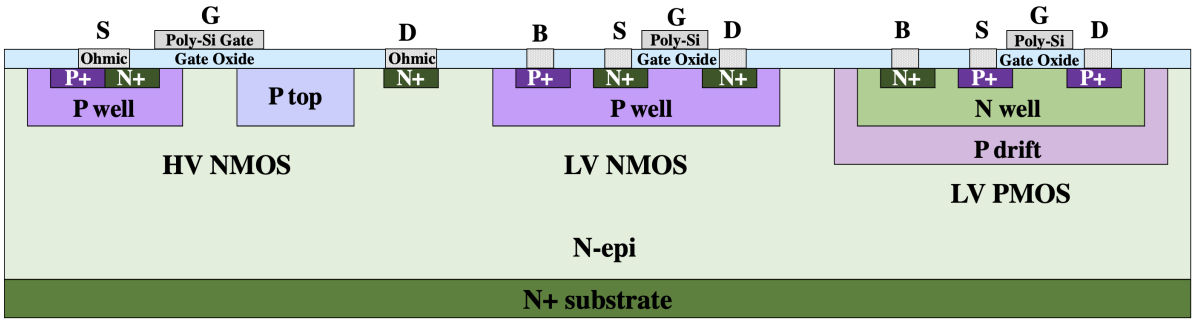

Fig. 1. Cross-sectional views of the HV NMOS, LV NMOS, and LV PMOS on the N-epi/N+ substrate are shown.

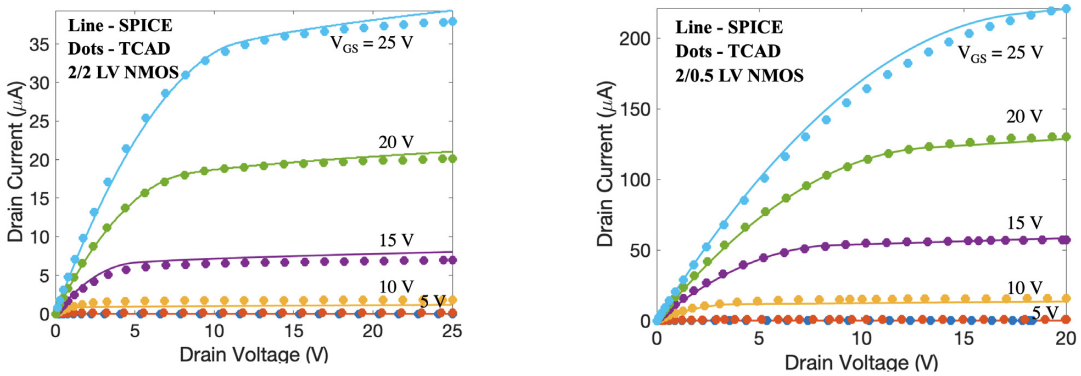

Fig. 2. TCAD-simulated (dots) and SPICE-simulated (solid lines) output characteristics of a 2 μm/2 μm (left) and 2 μm/0.5 μm (right) SiC LV NMOS.

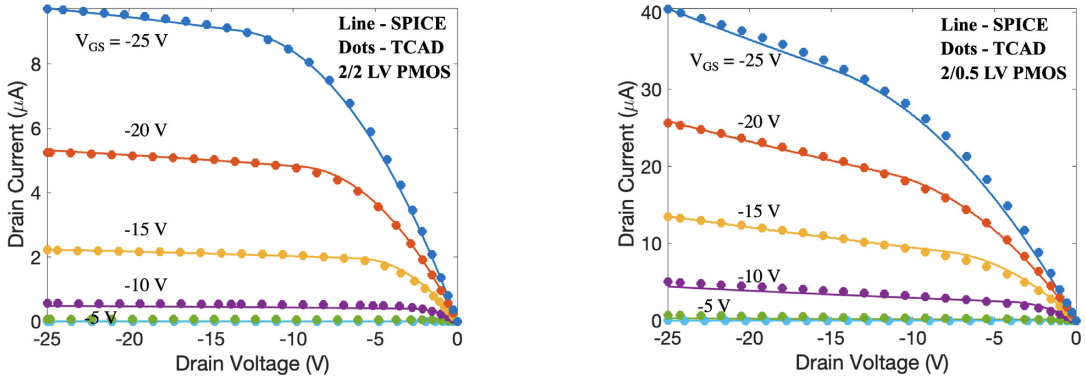

Fig. 3. TCAD-simulated (dots) and SPICE-simulated (solid lines) output characteristics of a 2 μm/2 μm (left) and 2 μm/0.5 μm (right) SiC LV PMOS.

gate oxide thicknesses are $50\,\mathrm{nm}$ for all MOSFETs. The single Reduced Surface Field (RESURF) technique [16] is utilized for the HV NMOS to manage the surface electric field and have a blocking voltage of over 600 V.

The expected electron and hole mobilities are $20\,\mathrm{cm^2\,V^{-1}\,s}$ and $5\,\mathrm{cm^2\,V^{-1}\,s}$, respectively. The well doping concentrations of the LV NMOS and LV PMOS are adjusted so that the threshold voltages are around 6 V for both types of LV MOSFETs. The maximum supply voltage is set at $25\,\mathrm{V}$. More comprehensive details regarding the device design and fabrication are included in [17]. Different types of 2-D simulations (shown in Table. I) are conducted to provide the necessary results for SPICE parameter extractions and model development (discussed in the next section).

III. SPICE Modeling

This section introduces the level 2 SPICE model and demonstrates the static performances of the developed level 2 SPICE models for the LV NMOS, LV PMOS, and HV NMOS. The level 2 SPICE model is a physics-based model with empirical parameters for improving the simulation accuracy. It is based on the Shichman-Hodges model (level 1) with added secondary effects such as carrier velocity saturation and mobility dependence of the vertical electric field [18].

The threshold voltage at zero body bias (VTO), the bulk threshold parameter (GAMMA), the substrate doping (NSUB), and the surface potential (PHI) are extracted from an iterative process with Ids vs. Vgs results under different substrate biases [19]. The mobility-related parameters (UO, UEXP, and UCRIT)

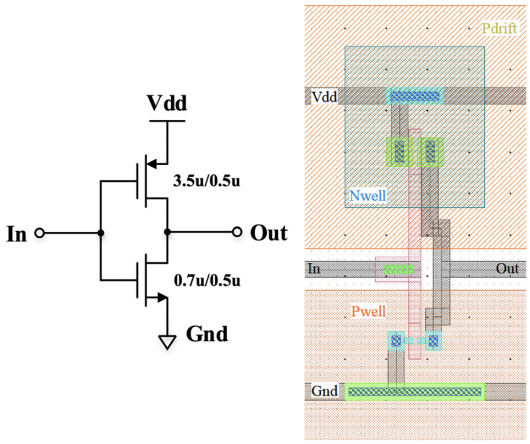

Fig. 4. Schematic (left) and layout (right) of the SiC CMOS inverter.

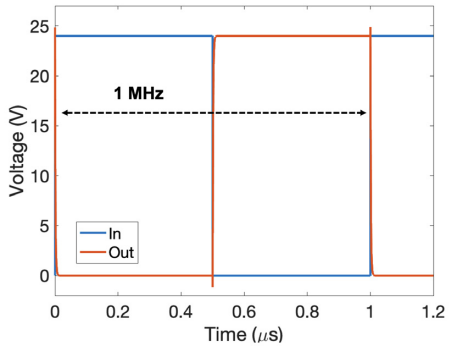

Fig. 5. Dynamic simulation of the SiC CMOS inverter with a 1 MHz input.

are extracted from the same data set. The channel length modulation (LAMBDA), carrier saturation velocity (VMAX), and depletion charge reduction parameter (NEFF) are extracted from the Ids vs. Vds simulations. Level 2 SPICE models are constructed based on the extracted parameters. Comparison between the SPICE simulations and TCAD simulations for selected NMOS and PMOS are presented in Fig. 2 and Fig. 3, respectively. High accuracy of the SPICE models is achieved for all types of MOSFETs. The developed SPICE models are incorporated into Cadence Virtuoso Analog Design Environment (ADE) for circuit simulations.

IV. Circuit Development and Simulation

In this section, the SPICE simulations of a SiC CMOS inverter and a SiC ring oscillator are presented to demonstrate the proposed technology. The design considerations, simulation results, and the corresponding layouts of the two types of circuits are discussed.

A. SiC CMOS Inverter

Fig. 4 shows the schematic and layout design of a SiC CMOS inverter. Minimum channel length (0.5 μm) is applied to both transistors and the minimum channel width (0.7 μm) is used

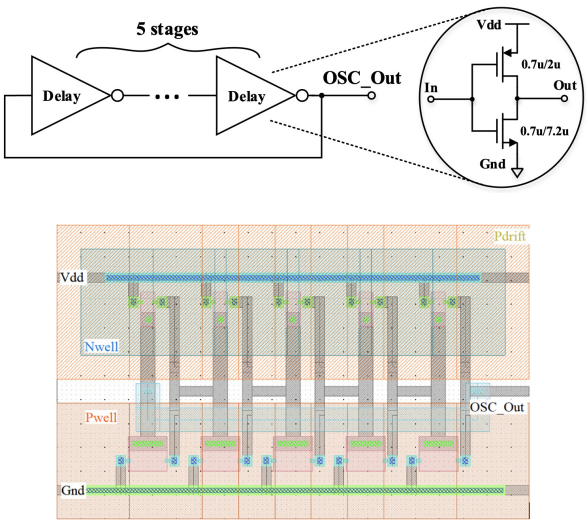

Fig. 6. Schematic (top) and layout (bottom) of the the 5-stage SiC ring oscillator.

for the LV NMOS to optimize the delay time. The width of the LV PMOS is sized to be five times the width of the LV NMOS to have identical rise time and fall time. This ratio is determined by the expected electron mobility ($20\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$) and hole mobility ($4\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$) in the channel. The inverter is simulated with a V_{dd} of 24 V and an input square signal of 1MHz, and the transient simulation result is shown in Fig. 5. The simulated rise and fall time is $3.2\,\mathrm{ns}$.

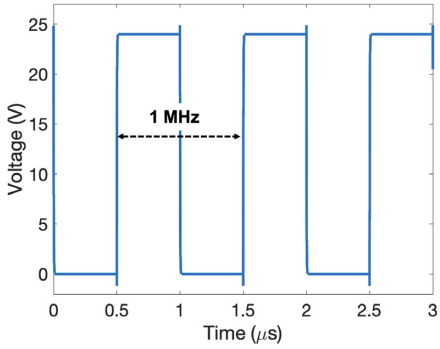

Fig. 7. Dynamic simulation of the SiC ring oscillator.

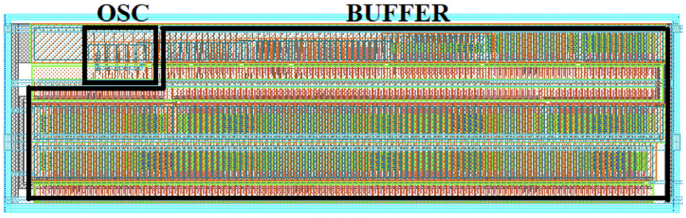

Fig. 8. Complete layout of the SiC ring oscillator with the buffer stage.

B. SiC Ring Oscillator

A ring oscillator is usually implemented to generate the on-chip clock signal. Fig. 6 shows the schematic and layout designs of a 1MHz SiC ring oscillator. The LVNMOS and LPMOS in each delay cell are sized as $0.7\mu m/7.2\mu m$ and $0.7\mu m/7.2\ \mu m$ to achieve $100\,\mathrm{ns}$ delay time and the identical rise/fall time. The ring oscillator is simulated with a $\mathrm{V_{dd}}$ of 24V, and the output signal is demonstrated in Fig. 7, showing a 1MHz oscillating frequency. To drive the parasitic capacitance of probing pads ($\sim$100pF), a buffer, which is a tapered inverter chain, is cascaded with the oscillator. The layout of the buffered oscillator is shown in Fig. 8.

The inverter and oscillator designs are sent out for fabrication. Characterizations of the fabricated circuits will be reported in future publications.

V. Summary

Level 2 SPICE models are developed for a SiC power IC technology that offers monolithic integration between high-voltage SiC power MOSFETs and low voltage SiC CMOS devices. Based on 2-D device simulations, accurate fittings are achieved for the developed SPICE models of the low-voltage NMOS and PMOS with different channel lengths. The models are integrated into Cadence Virtuoso Analog Design Environment for circuit simulations. Dynamic simulations and layout designs of a SiC CMOS inverter and a SiC ring oscillator are presented. The authors have sent out the inverter and the oscillators for fabrication.

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