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Development of Isolated CMOS and HV MOSFET on an N^-epi/P^-epi/4H-SiC N^+ Substrate for Power IC Applications

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***Abstract*— This paper reports the design and process flow of a fully integrated yet isolated low-voltage (LV) CMOS with high voltage (HV) lateral power MOSFET on a 6-inch 4H-SiC substrate for the development of HV SiC power ICs. The epi stack (N^-epi/P^-epi on N^+ substrate) for the development of the power ICs was optimized to accommodate and isolate the HV devices and circuits from their LV counterparts. The devices reported in this work were fabricated at 150mm, production grade-Analog Devices Inc. (ADI) Hillview fabrication facility located in San Jose, CA. The HV lateral NMOSFET from this work demonstrated a breakdown voltage (BV) of 620V and a specific on-resistance ($R_{on,sp}$) of 9.73 mΩ·cm² at gate-source voltage (V_{gs}) of 25V. A single gate oxide and ohmic process were used to fabricate the HV NMOS and LV CMOS devices and circuits. Junction isolation was implemented for isolating the HV and the LV blocks for the design of HV Power ICs. Finally, this work executed an HV capable three-metal layered back-end-of-the-line (BEOL) process, an imperative provision for developing reliable and robust power ICs. For future high-temperature applications, the static performances of the devices are characterized and are reported up to 200°C.**

Keywords*— *4H-SiC, lateral MOSFET, RESURF, CMOS, Power IC

I. Introduction

Over the decades, Si-based power and microelectronic CMOS devices have been the affirmative technology for power conversion but are limited in terms of power processing capability. SiC-based electronics not only allow improved high-power conversion but also enable high-temperature operation due to its superior material properties when compared to its Si counterparts. SiC power ICs have potential applications in HV power management ICs, DC-DC converters for distributed power resource systems, onboard charging for electric vehicles (EV's), power supplies for high-performance servers and battery management ICs. In the modern-day scenario, Si-based ICs drive the discrete SiC power MOSFETs which appends to increase in size, cost, parasitic effects in interconnections, and hence reduction in reliability. So, to contend the above concerns, there is a demand for the development of SiC-based single-chip solution (SiC power ICs) that provides both power and control capability, significantly simplifying system-level designs. The eventual goal of this work funded by ARPA-E is to demonstrate fully integrated HV SiC Power MOSFET ICs [1]. As an initial stride in achieving that landmark, the HV Power NMOS and LV CMOS are monolithically integrated on a 6-inch N^-epi on N^+ substrate using a single process flow as shown in Fig. 1 and reported in [2]. Although in [2], the HV and LV components are monolithically integrated, they all share the same conducting N^+ substrate thereby lacking the isolation which is a significant requisite in developing HV Power ICs on a single chip as shown in Fig. 1. Accordingly, moving one step forward, the epi stack in this work has been modified and optimized such that the HV blocks (HV NMOS and LV-HV Bulk) are completely isolated yet integrated with the LV CMOS as shown in Fig.2. P^+ Isolation in conjunction with P-epi is used to isolate the LV from HV blocks. Similar to [2], a single gate oxide and ohmic process are used to integrate the HV and LV CMOS devices. Finally, this work incorporates an advanced back-end-of-the-line (BEOL) process with three metal layers, offering an edge in flexible metal routings and in developing scalable Power ICs.

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II. Fabrication Process

Fig. 2 shows the cross-section of the fabricated HV NMOS, LV NMOS, and LV PMOS structures on a 6-inch N^-epi/P^-epi on N^+ substrate. A 2.5 µm thick, 6.5 × 10^{16} cm^{-3} doped N^-epi layer and 6 µm thick, 2 × 10^{16} cm^{-3} doped P^-epi layer on N^+ substrate was used as the starting material.

A. N and P layers using Ion Implantation

The N Well and N^+ source/drain were formed using Nitrogen ion implants. P Well, P^+ source/drain, and P top are implemented using aluminum ion implants. The deep junction P^+ Isolation was formed by aluminum channeling implantation. Followed by the ion implantation process, the wafers were annealed at 1650°C for 10min with a carbon cap to activate the implanted aluminum and nitrogen ions.

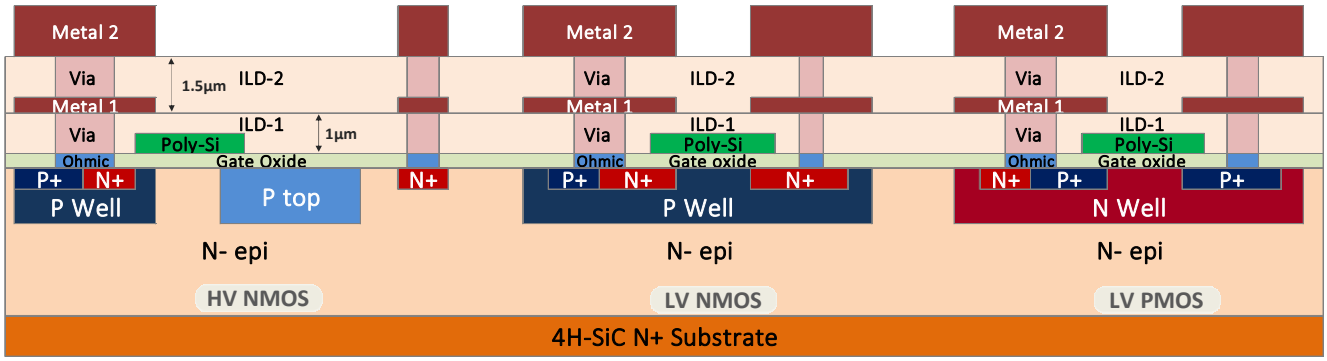

Figure 1: Cross-section of the fabricated HV NMOS, LV NMOS and LV PMOS on an N-epi grown on N+ substrate [2].

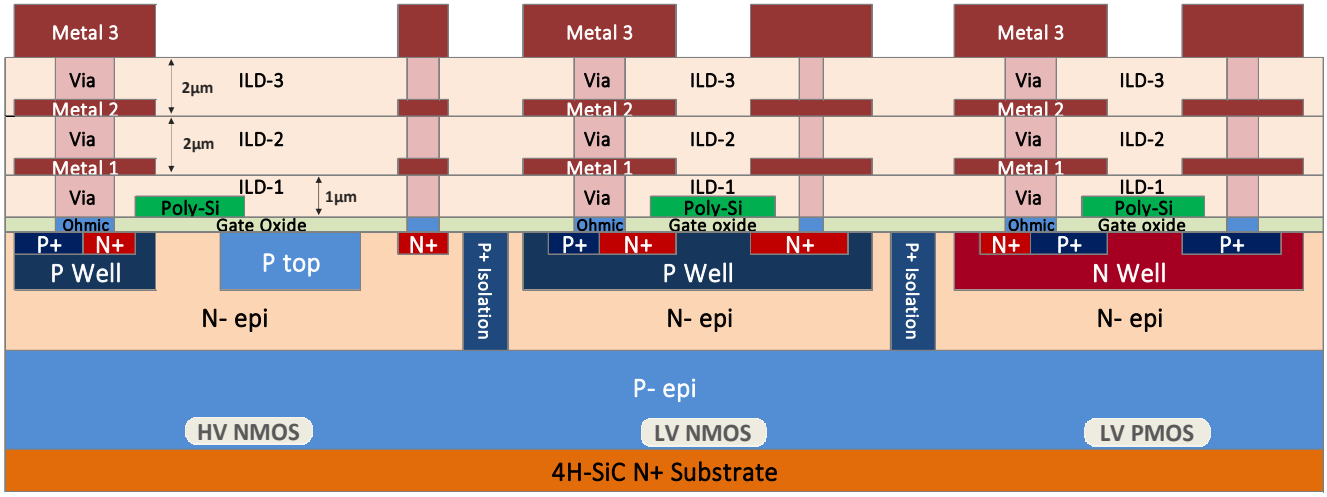

Figure 2: Cross-section of the fabricated HV NMOS, LV NMOS, and LV PMOS on an N^-epi/ P^-epi grown on N^+ substrate; P+ Isolation pillars shown in the figure are used for isolation of HV and LV devices.

B. Gate Oxide and Gate Poly formation

A single gate oxide recipe was developed for both NMOS and PMOS to achieve maximum channel mobilities and better dielectric quality. A 50 nm thick gate oxide was formed with high-temperature CVD oxide. Post Oxidation annealing (POA) was performed for 180 min in N_2O and N_2 atmospheres. Once gate oxide was formed, 0.5 µm gate polysilicon was deposited, doped with phosphorous, and patterned.

C. Ohmic and Three metal layer process

Followed by the gate formation, a first interlayer dielectric (ILD-1) of thickness 1µm was deposited and etched for ohmic contacts. N-type and P-type ohmic contacts were formed concurrently using a single ohmic metal (Nickel). 1000 Å Nickel was deposited on the front side, followed by annealing at 750°C for 2 min to form Nickel silicide and further annealing at 965°C for 2 min. Ohmic contact was also formed on the backside of the wafer. A 0.5 µm thick Aluminum metal (metal 1) was deposited, patterned, and etched. The second layer of 2 µm ILD-2 was deposited and followed by planarization using CMP. The ILD-2 was etched for Via and filled with W-based metal. Another 0.5 µm thick Aluminum metal (metal 2) was deposited, patterned, and etched. The third layer of 2 µm ILD-3 was deposited similar to ILD-2. The ILD-3 was etched for Via and filled with W-based metal similar to the earlier vias. The topside metal of 4.5 µm thick Aluminum (metal 3) was deposited, patterned, and etched. Finally, the surface was passivated by silicon nitride and polyimide.

III. Electrical Characteristics of Devices and Test Structures

In this section, the designs and electrical performances of the fabricated devices and test structures are discussed. Firstly, Section-A discusses the design and electrical performances of the HV Power NMOSFET followed by NMOS and PMOS in section-B. Section-C discusses the gate dielectric quality of this work. The extracted electron and hole channel mobilities from the test structures are discussed in section-D. In section-E, the inter-metal dielectric (ILD) breakdown of this fabrication technology is reported. Finally, the verification and junction isolation voltage blocking capability are reviewed in section-F.

A. HV NMOSFET

The HV NMOS is designed based on the REduced SURface Field (RESURF) concept. The surface Al implanted P

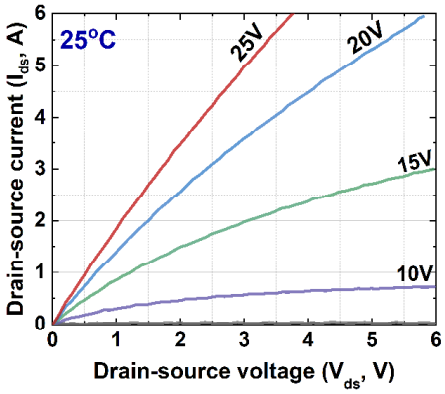

Figure 3: Typical output characteristics of the HV NMOS at 25°C.

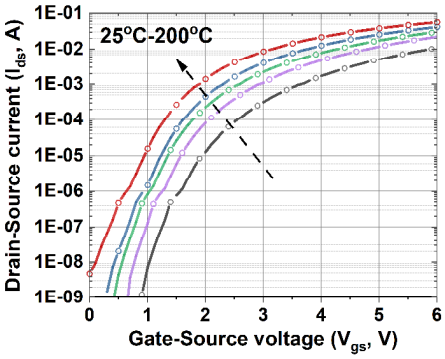

Figure 4: Typical transfer characteristics of HV NMOS at various temperatures.

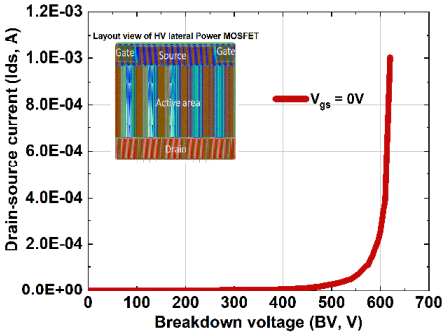

Figure 5: Measured blocking characteristics of HV NMOS at 25°C.

top and the bottom P- epi collectively form the double RESURF to suppress and uniformly distribute the electric field thereby enhancing the breakdown voltage. The critical parameters of HV NMOS in this work are similar to our previously reported design in [2].

Fig. 3 shows the typical on-wafer output characteristics and the extracted $R_{on,sp}$ of the HV NMOS at gate-source voltage (V_{gs}) of 25V is 9.73 mΩ·cm^2 at 25 °C. The transfer characteristics of the HV NMOS are shown in Fig. 4. The threshold voltage at I_{ds} of 100 µA is about 2.6 V at 25°C. Fig. 5 shows the measured blocking characteristics of the HV NMOS demonstrating a breakdown capability of 620V in the lateral direction at I_{ds} of 1mA and V_{gs} of 0V.

B. LV CMOS

The LV NMOS is formed by P Well, N^+ source, and drain implants. The P Well of the LV NMOS has the same design as

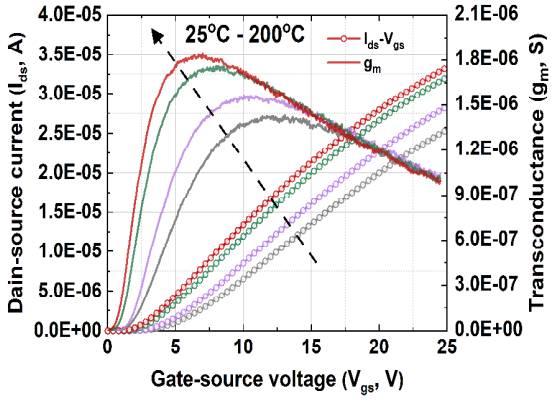

Figure 6: Transfer characteristics of LV NMOS ranging from 25°C to 200°C.

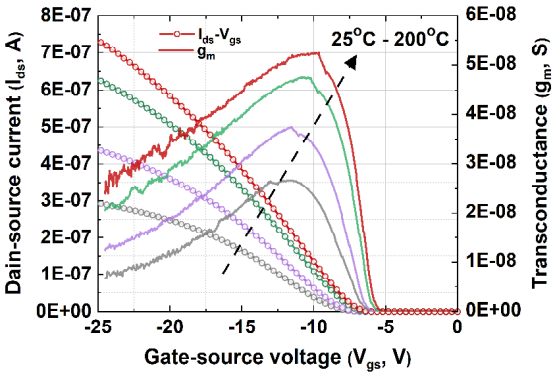

Figure 7: Transfer characteristics of LV PMOS ranging from 25°C to 200°C.

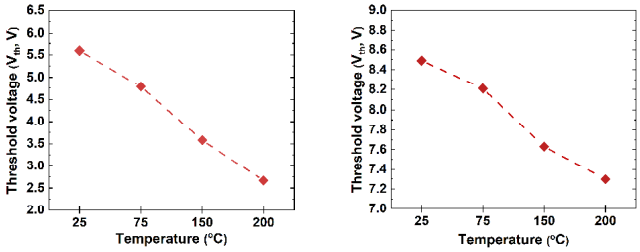

Figure 8: Vth variation of LV NMOS (left) PMOS (right) across 25°C to 200°C.

the P Well optimized for the HV NMOS. The P Well is designed to form an accumulation mode channel with a surface n-channel doping of 6.5 × 10^{16} cm^{-3}. Moving onto LV PMOS, it is formed by the N Well, P^+ source, and drain implants. The N Well is also designed to form an accumulation channel with a surface p-channel doping of 2 × 10^{17} cm^{-3}, intended to achieve a lower threshold voltage. The typical transfer characteristics of the 10 µm wide and 1 µm long LV NMOS and 10 µm wide and 10 µm long LV PMOS across 25°C to 200°C are shown in Figs. 6 and 7, respectively. Using the linear extrapolation method, the threshold voltages of LV NMOS and LV PMOS were extracted at maximum value of transconductance. The extracted threshold voltages and its variation across 25°C to 200°C for LV NMOS and LV PMOS are shown in Fig. 8. The threshold voltages of both NMOS and PMOS exhibit a negative temperature coefficient due to the reduction in the electrons trapped in the interface states with the increase in temperature. The typical I-V characteristics of the LV NMOS and LV PMOS are also shown in Figs. 9 and 10, respectively at 25°C, 150°C and 200°C.

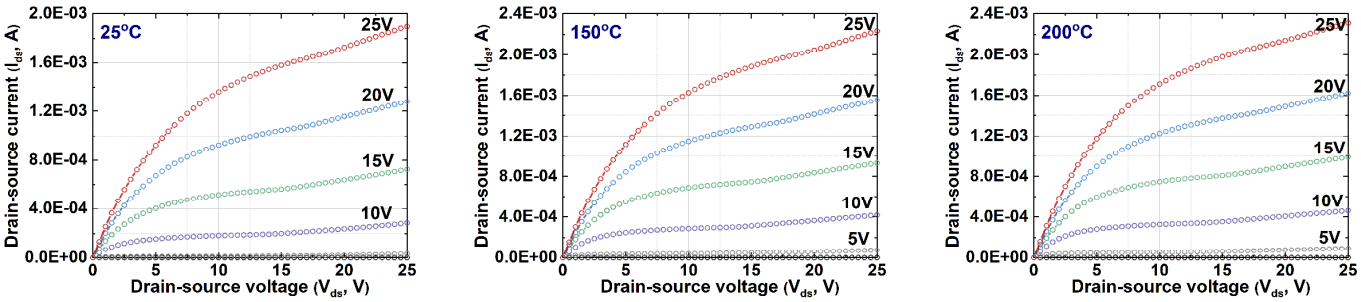

Figure 9: Output characteristics of 10 µm wide, 1 µm long LV NMOS at 25°C, 150°C, and 200°C.

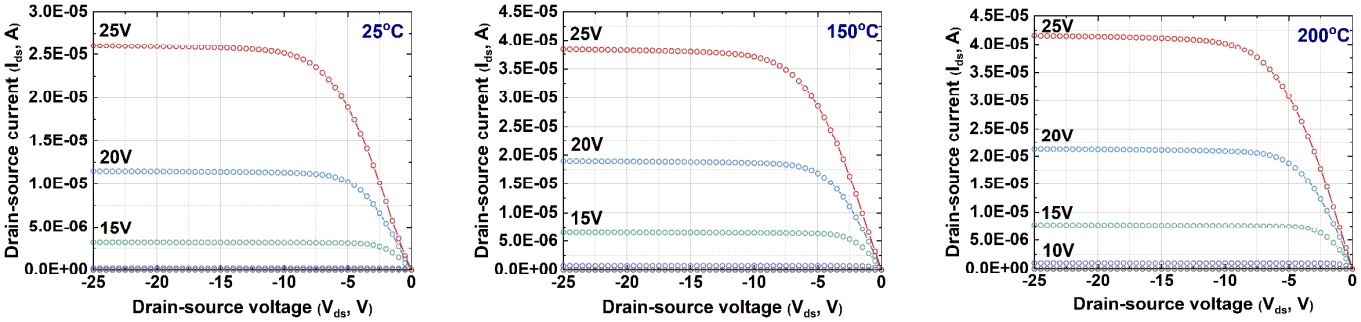

Figure 10: Output characteristics of 10 µm wide, 10 µm long LV PMOS at 25°C, 150°C, and 200°C.

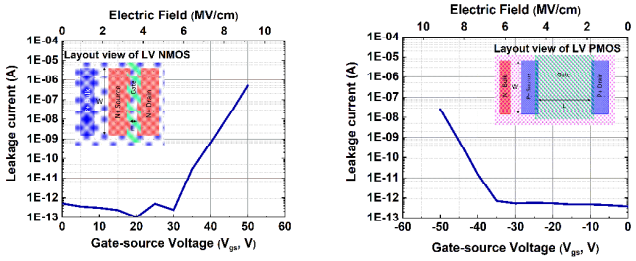

Figure 11: Gate-source breakdown of LV NMOS (left) and LV PMOS (right)at 25°C.

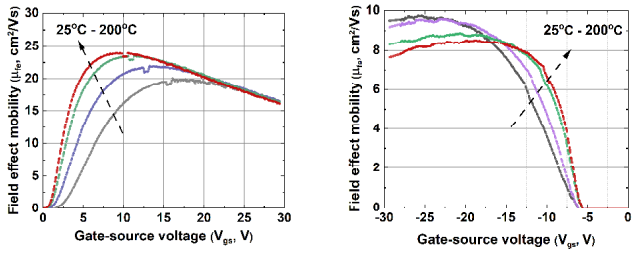

Figure 12: Field effect mobilities of electrons (left) and holes (right) at 25°C to 200°C.

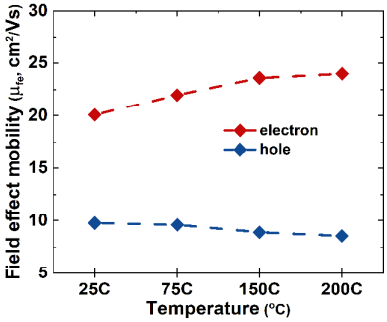

Figure 13: Summary of peak mobility variation of electrons and holes over 25°C to 200°C.

C. Gate dielectric quality

The gate oxide dielectric quality of this work is evaluated on the LV NMOS and LV PMOS. The gate-source leakage currents of the NMOS and PMOS are extracted at 25°C. Both NMOS and PMOS showed relatively low gate-source leakage current demonstrating a high breakdown field above 9 MV/cm and accordingly a superior dielectric quality as shown in Fig. 11.

D. Electron and Hole Field effect mobilities

The field-effect mobilities of electrons and holes are extracted from 200 µm x 200 µm FATFET structures. Both the n-FATFETs and p-FATFETs in this work have an accumulation channel. The surface n-channel doping for n-FATFET is about 6.5×10^{16} cm^{-3} while the p-channel doping for p-FATFET is 2×10^{17} cm^{-3}. Fig. 12 shows the field-effect channel mobilities of electrons and holes ranging from 25°C to 200°C. The peak electron mobility at 25°C is about 20cm^2/V·s while peak hole mobility is about 9.77cm^2/V·s. The peak mobilities of electrons and holes across the temperature range is summarized in Fig. 13.

E. Interlayer Dielectric (ILD) breakdown

Having a multi-layered metal scheme is a compelling asset to develop robust, scalable, and reliable HV power ICs. However, it is significant that the interlayer dielectric between the metal layers should withstand high voltages. This work implements a three-metal layer scheme with a 1.5 µm thick dielectric material between them as shown in Fig. 2. A metal-insulator-metal (MIM) capacitor that's formed between Metal 2 and Metal 3 was measured to demonstrate the ILD breakdown capability. The 1.5µm ILD between Metal 2 and Metal 3 has demonstrated a voltage capability as high as 900V with 1nA leakage and a breakdown field of 9MV/cm between metal layers as shown in Fig. 14.

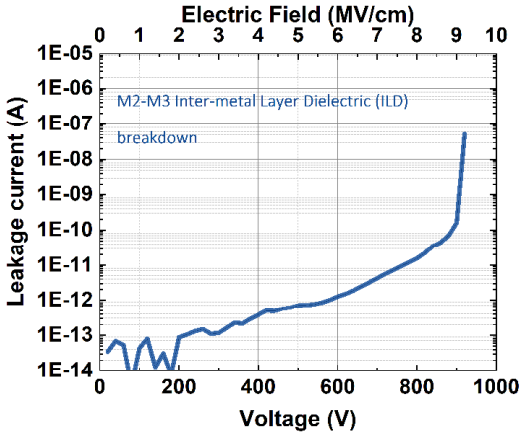

Figure 14: 1.5µm ILD breakdown across Metal 2 (M2) and Metal 3 (M3).

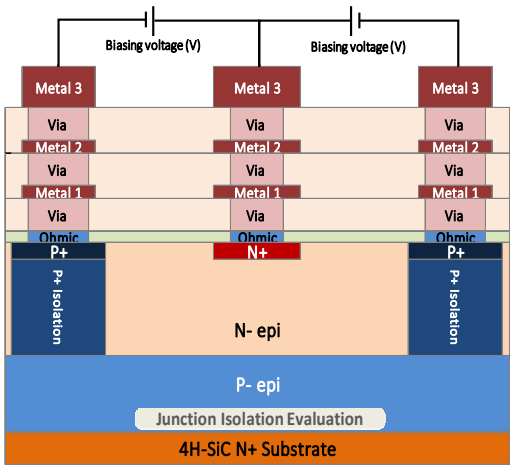

Figure 15: Test structure to verify the junction isolation voltage blocking capability.

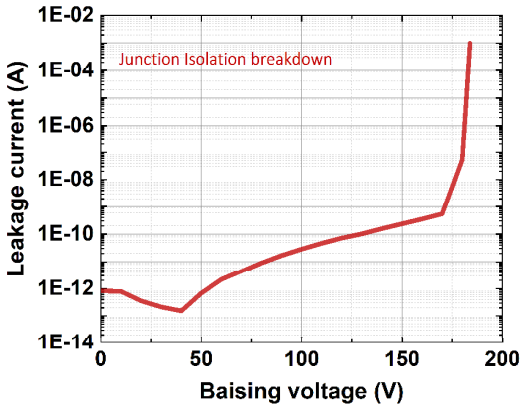

Figure 16: Junction Isolation voltage blocking capability.

F. Junction Isolation voltage blocking capability

For the development of single-chip HV Power ICs solutions, isolation of LV entities from HV devices is indispensable. Junction isolation was adopted in this work to shield the LV blocks from high voltages. As shown in Fig.15, P+ Isolation in conjunction with P-epi is used to isolate the potential of the N-epi with another. The P+ Isolation shows a blocking capability of 180V as shown in Fig. 16, justifying the effectiveness and voltage blocking capability. The junction isolation was further optimized to increase the blocking capability which will be reported in our future work.

IV. Conclusions

Successful demonstration of isolated yet integrated LV CMOS and HV Power MOSFET on a 6-inch N^-epi/P^-epi on N^+ substrate for Power ICs applications and development. A single process flow has been developed to extract optimum performances from LV and HV devices. The significant electrical characteristics of the HV Power MOSFET and LV CMOS devices and test structures have been reported up to 200°C. Based on the demonstrated fabrication technology and design methodology a performance enhanced SiC power MOSFET along with HV Power IC will be reported in the future.

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