# Design Strategies for Rugged SiC Power Devices

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***Abstract*—This paper focuses on the design strategies for achieving adequate ruggedness of silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs). Currently available 1200 V MOSFETs from various vendors show a big variance in short circuit time, threshold voltage shift, and gate leakage currents. The short circuit (SC) test of three commercial TO-247 packaged MOSFETs with voltage ratings of 1200 V at room temperature show that the SC times are much lower than silicon devices. Threshold shifts under rated DC positive gate bias up to 100 hrs vary from 0.1 V to 0.5 V for different vendors. Fowler-Nordheim (FN) tunneling currents were measured as a function of gate bias and junction temperature. The FN gate leakage currents and temperature dependence are markedly different for various vendors. One vendor (for devices E and E') stands out for best performance in all three respects.**

**Index Terms-*Short circuit, failure mechanisms, threshold voltage stability, Fowler-Nordheim tunneling, SiC- MOSFETs***

## I. Introduction

Silicon carbide (SiC) devices have great potential for high voltage, high power density and high frequency applications due to higher bandgap energy, breakdown field, and thermal conductivity [1]. In recent years, the SiC power metal-oxide-semiconductor field-effect transistors (MOSFETs) have been demonstrated in a wide range of applications such as modular multilevel converter (MMC) based high power motor drives [2], high efficiency photovoltaic harvesting systems [3], and high power density inverter for electrical vehicles (EV) [4]. Since SiC MOSFETs are now widely available from several commercial venders, the ruggedness of these commercial SiC MOSFETs is critically important for adoption in applications.

During normal operation, the switching devices are required to sustain short circuit (SC) events at high drain-to-source voltage with full applied gate voltage for short periods. Automotive inverters for hybrid or electric vehicles demand longer SC time due to locked rotor and climb events in a normal drive cycle. During over-current caused by short circuit fault, the desaturation circuits are able to protect the devices within 10 µs [5]. It is desirable for the commercial SiC devices to have the 10-µs SC sustaining capability similar to the Silicon counterparts, in the event of a SC fault. Therefore, it is necessary to characterize the devices' SC withstanding capability and subsequent degradation. Similarly, it is very critical to have threshold voltage stability under positive and negative gate bias and high enough threshold voltage to handle inductive gate bounce during circuit operation. The gate leakage current at high junction temperatures is also critical for automotive applications.

TABLE I. TESTED DEVICES

| Device | Material | Voltage Rating | Current Rating | Approximate Die Size |
|---|---|---|---|---|
| A | Si | 900 V | 5 A | 7.85 mm² |
| B | SiC | 900 V | 11.5 A | 1.89 mm² |
| C | SiC | 1200 V | 12 A | 3.85 mm² |
| D | SiC | 1200 V | 14 A | 3.96 mm² |
| E | SiC | 1200 V | 32 A | 8.48 mm² |

## II. Test Results and Discussion

### A. Short Circuit Test Results

This paper reports the SC test results of five commercial MOSFETs as shown in Table I. The high saturation current density at high drain bias results in reduction of SC time due to increased heat dissipation under short circuit conditions. The heat generation per unit die area in SiC devices under SC condition is much higher than Si devices due to smaller die area of SiC devices for similar on-resistance. It should be noted that the SC condition for 10-15 µs is an adiabatic event where the heat is stored in the die raising its temperature and does not have enough time to dissipate through the package and to the heatsink.

Fig. 1(a) shows 1-µs pulse waveforms for the 1200-V SiC MOSFET (E). The 1-µs time was chosen to avoid excessive heating during the pulse. Despite this precaution, due to high heat dissipation, the temperature of the die rises during the 1-µs pulse. Initially the device current increases due to RC time constant associated with gate charging and increase of inversion layer electron mobility with temperature [6] and then reduces due to net reduction in inversion layer and bulk electron mobilities at higher temperatures. The saturation current value was measured at the peak current point during the 1-µs turn-on period. In contrast, the Si MOSFET, as shown in Fig. 1 (b), does not exhibit heating due to much lower current and bigger die area.

Fig. 2 compares $J_{ds}$-$V_{ds}$ characteristics of all the devices in Table I when they are fully turned on at full gate voltage and 600-700 V drain voltage. This data was collected with 1-µs gate pulse to avoid excessive heating as described above. It shows that the SiC MOSFETs conduct much higher current densities in the saturation region as compared to the Si MOSFET due to very short channel lengths used to overcome the limitation of low inversion layer mobility. According to Fig. 2, SiC devices B and E would generate the highest heat dissipation per unit area under short-circuit. The Si MOSFET

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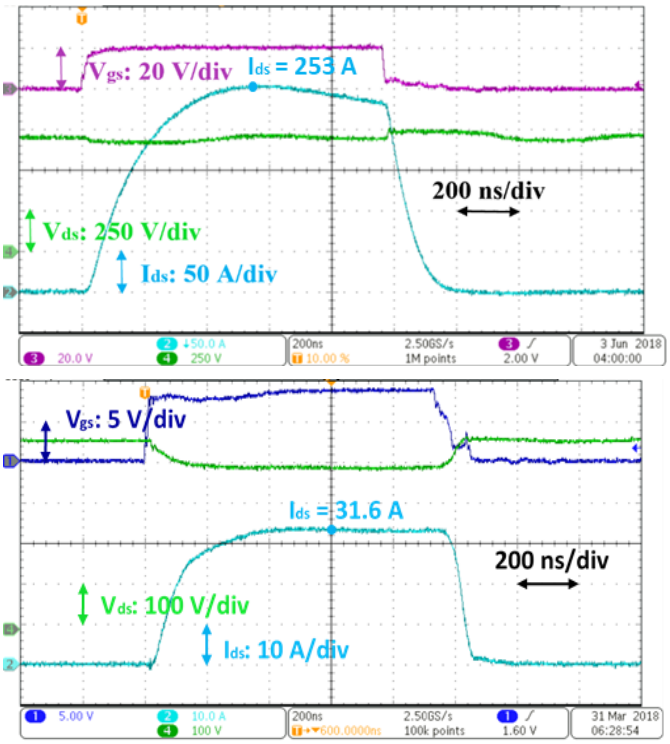


Fig. 1. The device switching waveforms with 1-µs gate voltage pulse at room temperature. (a) The 1200-V SiC MOSFET (E) with $V_{gs}$ = 20 V and $V_{ds}$ = 675 V; (b) The 900-V Si MOSFET (A) with $V_{gs}$ = 9 V and $V_{ds}$ = 400 V.

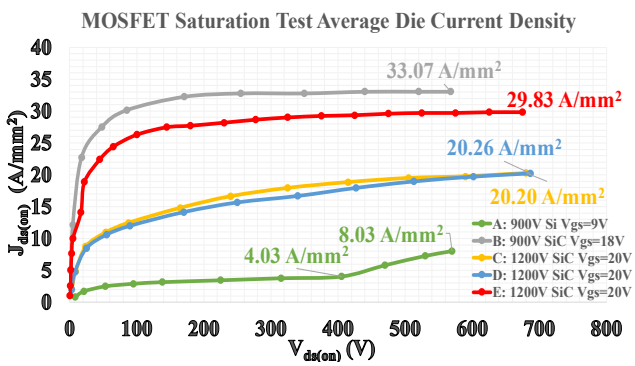


Fig. 2. 1st-quadrant $J_{ds}$-$V_{ds}$ curves with maximum rated gate voltage and high drain voltage for the five devices in Table I.

would have the least amount of heat generated per unit area under short-circuit and therefore should have the longest SC time. The Si MOSFET shows an increase in saturation current for $V_{ds}$ greater than 400 V. The potential mechanism may be related to the parasitic npn bipolar junction transistor (BJT) in the Si MOSFET.

A typical SC test for pulse width of 10 µs is shown in Fig. 3 for SiC device B in Table I. Measurements are done at different values of drain voltage, $V_{ds}$, while applying the full rated gate voltage, $V_{gs}$. The device heats up over 10 µs. After initial rise in current due to RC time constant associated with gate charging and increase of inversion layer electron mobility with initial rise in temperature to about 150°C, the current reduces due to reduction in electron mobility in the inversion

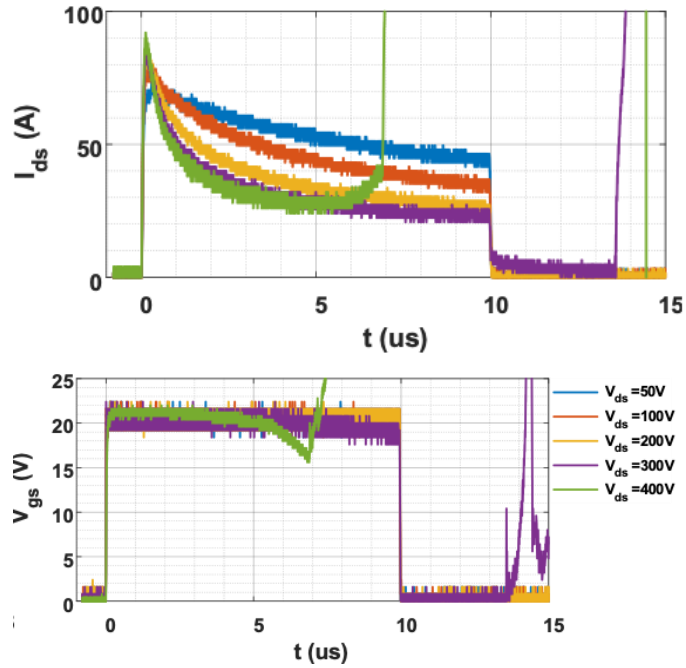


Fig. 3. Short circuit tests on Device B, 900 V SiC MOSFET.

Table II. Short Circuit Test Results

| Tested device | Max 10-µs SC sustaining voltage | Average Die power density (kW/mm²) at 300-V $V_{ds}$ over 10 µs |
|---|---|---|
| A: 900 V 5.1 A Si | 400 V to 500 V | 0.99 |
| B: 900 V 11.5 A SiC | Around 300 V | 5.14 |
| C: 1200 V 12 A SiC | Around 400 V | 3.71 |
| D: 1200 V 14 A SiC | Over 600 V | 4.90 |
| E: 1200 V 32 A SiC | 500 V to 600 V | 5.30 |

layer and drift layer with further increase in temperature. The higher drain voltages result in higher heat dissipation which stays in the device active layer for 10 µs. Eventually, at some drain voltage, the device is destroyed due to excessive heating. Device B develops a gate-short due to high temperature at high drain voltage (400 V) presented as a dip in the $V_{gs}$ waveform and is thermally destroyed. Most of the commercial devices use Al as overlayer which melts at 660°C and presumably destroys the device. One strategy for improving the short circuit time of SiC devices would be to use an overlayer with higher melting point such as Copper (1084°C), Platinum (1770°C) or Molybdenum (2620°C) or suitable alloys.

Table II summaries the test results for the five devices. The second column shows five devices' possible largest sustaining voltages without a failure up to 10 µs. The third column shows the average die power density at 300-V $V_{ds}$ over 10 µs. This was calculated by integrating $J_{ds}$ vs $V_{ds}$ curves over 10 µs, dividing by 10 µs and then multiplied by 300 V. The average power density during short-circuit measurement is between 3.70 to 5.30 kW/mm2 (discounting the Si device) which is significantly higher than what is

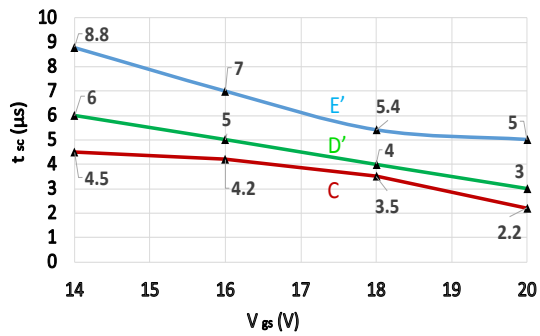


Fig. 4. SC time as a function of gate voltage at $V_{ds}$ = 800 V. Device D' is the same vendor D in Table I but with rating of 1200 V, 17A. Device E' is the same vendor E in Table I but with rating of 1200 V, 10 A.

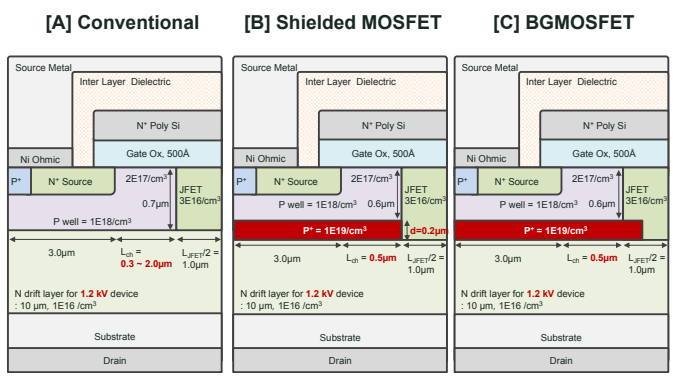


Fig. 5. (a) Conventional SiC MOSFET, (b) Shielded MOSFET and (c) Buffered Gate (BG) MOSFET structures.

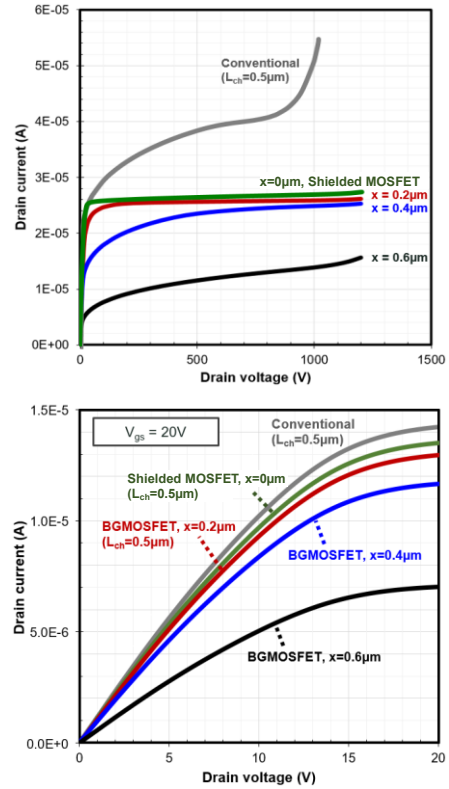


Fig. 6. Simulated I-V characteristics of the three SiC MOSFET structures with channel length of 0.5 µm and VG = 20 V at (a) high drain voltages showing output current and (b) low drain voltages showing on-resistance. Dimension x refers to extension of p+ shield into the JFET region.

observed during nominal operation. This explains why the temperature rise is much higher in SiC devices compared to silicon during a short-circuit event. Assuming similar dielectrics and overlayer metals are used in both Si and SiC devices, it is understandable that SiC devices would have much shorter SC times as compared to Si devices.

Another possible strategy to improve the SC time is to reduce the operating gate voltage. The data in Fig. 4 shows the SC time for 1200 V devices from 3 different vendors. The data was taken at drain bias of 800 V. This data is very useful for circuit designers and allows the selection of SC time by using appropriate gate voltage. It should be noted that the reduction of gate voltage will result in an increase in on-resistance of the device. This represents a typical trade-off between cost and ruggedness.

Some design changes within the device can be considered to improve the SC time. Fig. 5 shows the cross-section of three different device designs considered, each with a channel length of 0.5 µm. For the conventional design Fig. 5(a), a physics-based two-dimensional device simulator (Atlas) confirmed that a short-channel device resulted in higher output conductance as shown in Fig. 6(a), which would increase the SC current at high drain voltage, thus resulting in very low SC times. Figs. 5(b) and 5(c) depict two other designs that have been investigated—a shielded MOSFET [7] and a buffered-gate (BG) MOSFET [8], respectively. Shielded MOSFETs have a *p*+ region of 0.2 µm thickness with very high *p*-type doping concentration of $N_A = 10^{19}$ cm$^{-3}$ at the bottom of the *p*-well. The BG MOSFET has a *p*+ region $N_A = 10^{19}$ cm$^{-3}$, which extends into the JFET region from 0.2 to 0.6 µm. In both designs, the *p*+ region shields the electric field in the junction between channel and JFET regions, and affects the device on-resistance and saturation current at low and high drain voltages, respectively. Although the BG MOSFET with *p*-type extension had the lowest peak electric field (enhancing the shielding), the on-resistance of this device increased significantly as the extension distance *x* increased as shown in Fig. 6 (b). This is contrasted by the Shielded MOSFET, which offers both a low peak electric field in the JFET region and low saturation drain current at high drain voltages without compromising device on-resistance—making this the preferred device design.

A very novel method of reducing the short circuit current has been recently reported [9,10]. In this method, a small resistance is introduced in the n$^+$ source of SiC MOSFETs which reduces the effective $V_{gs}$ in proportion to the current flowing. At operating current level, this reduction in $V_{gs}$ is small resulting in a small increase in on-resistance while under short circuit conditions, it results in relatively large reduction in *Vgs* and thus effectively limiting the short circuit current. The source resistance can be built-in by reducing the n$^+$ doping or by other means including an external resistance. The value of this resistance has to be carefully optimized.

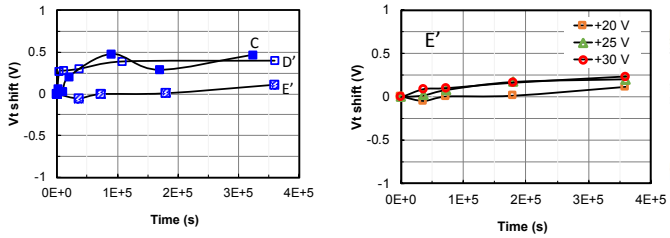


Fig. 7. (a) Threshold voltage shift over 100 hrs with $V_G$=+20 V stress, source and drain grounded at room temperature. Device D' is the same vendor D in Table 1 but with ratings of 1200 V, 17A. Device E' is the same vendor E in Table 1 but with ratings of 1200 V, 10 A. (b) Threshold voltage shift on device E' up to +30 V on the gate over 100 hrs.

## B. *Threshold Voltage Stability*

Threshold voltage stability, studied in this work is caused by a high density of traps and trapped charges at or near the interface of SiC/$SiO_2$ [11, 12]. Due to the existence of these traps, when a positive DC bias is applied to the gate over a long period of time, the threshold value shifts in the positive direction due to the capture of electrons by traps. Conversely, when a negative bias is applied to the gate over a long period of time, the threshold voltage shifts in the negative direction resulting in a significant increase in leakage current in the off-state. Furthermore, a negative shift of threshold voltage can cause devices to turn on unexpectedly and lead to failures.

In this work, the results of threshold voltage instability measurements of 1200 V 4H-SiC DMOSFETs from different vendors are reported. We investigate this particular trap-induced device degradation on commercially available devices by applying a positive voltage stress on the gate over a long period of time, with source and drain grounded. At the end of each stress, transfer characteristics ($I_D$-$V_G$) were measured to determine the threshold voltage shifts. The results are shown in Fig. 7 for $V_G$ = +20 V up to 100 hrs of stress at room temperature. Considerable variance between devices from different vendors was observed implying that while some vendors have been able to significantly reduce the near interface traps in the gate oxide, the others may still need some development. The device E' shows minimum shift (~0.1 V) at 20 V and only 0.25 V shift at 30 V up to 100 hrs. Clearly the vendor for E' has been able to reduce the near interface traps in the gate oxide.

## C. *Gate Leakage Current*

In order to have long-time reliability of the gate oxide of 4H-SiC MOSFETs, two major concerns should be investigated; Fowler-Nordheim (F-N) tunneling current and Time-Dependent Dielectric Breakdown (TDDB). It is worth noting that these measurements, have so far been performed on small area SiC MOS capacitors and no study on commercial 4H-SiC MOSFETs, to the author's knowledge, has been reported. Therefore, it is critically important to analyze the F-N tunneling current and TDDB on relatively large area commercial SiC MOSFETs at different temperatures to evaluate the current status of the gate oxide reliability of these devices and predict their ruggedness under realistic operations.

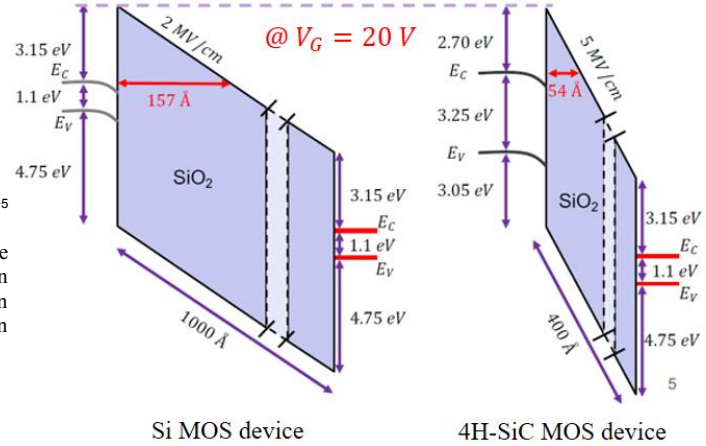


Fig. 8. Energy band diagrams of Si and 4H-SiC MOS devices at $V_G$ = 20 V. SiC MOS devices have a lower effective barrier height and thinner gate oxide than the Si MOS devices. The gate oxide thickness is assumed to be 100 nm and 40 nm for Si and SiC MOS devices. The F-N tunneling distance at 5 MV/cm in SiC MOS gate oxide is ~5.4 nm.

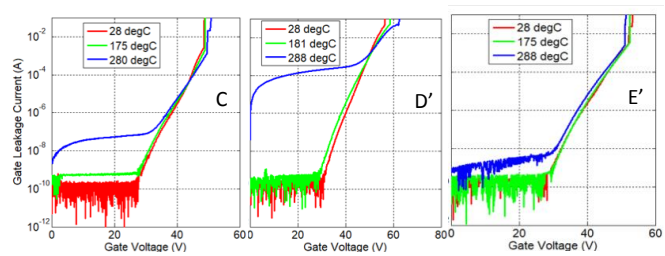


Fig. 9. Plot of gate leakage current vs. gate voltage in devices. Device D' is the same vendor D in Table I but with ratings of 1200 V, 17A. Device E' is the same vendor E in Table I but with ratings of 1200 V, 10 A.

Due to a lower effective barrier height and higher gate oxide electric field at the interface of SiC/$SiO_2$ compare to the Si/$SiO_2$ MOS system, electron tunneling probability into the gate oxide of 4H-SiC MOS devices is higher than the Si MOS devices (Fig. 8) [13]. Furthermore, the F-N injection of electrons into the gate oxide increases at elevated temperatures. The F-N tunneling current as a function of gate bias was measured by measuring the gate leakage current with the device under positive voltage and source and drain terminals grounded. The results are shown in Fig. 9. The quality of the gate oxide is indeed very good for vendor E' as we see a very clean F-N tunneling current which is well-behaved at higher temperatures. The increased leakage at low gate bias at elevated temperature is possibly the parasitic conduction in the package. The device E' shows the expected behavior at high temperature with reduction in breakdown voltage at higher temperature. Devices C and D' show anomalous behavior possibly due to mobile ion contamination either in the gate dielectric or the package.

# III. Conclusion

The short circuit tests were conducted on one silicon and four SiC MOSFETs. It can be inferred that none of the commercial SiC devices could sustain a 10-µs short circuit time at two third of rated drain-source voltage without

apparent degradation or failure. The primary reason is that the device size has been reduced significantly to reduce cost by reducing the channel length. Clearly, redesign of the devices is needed to improve the short-circuit time if warranted by the applications. The SC time may be improved by reducing the gate voltage or using a source resistance at the expense of the on-resistance. Shielded MOSFET structure represents a design approach to improve SC time. Also, different overlayer metal with melting point much higher than Al may be used. Wide variance in positive threshold shift due to application of rated gate voltage at room temperature is seen among various vendors. This indicates the presence of the so-called border traps. The devices E' exhibit only 0.1 V threshold shift under +20 V gate bias over 100 hrs. This vendor has significantly reduced the border traps in the gate oxide. The devices from the same vendor show very clean Fowler Nordheim gate leakage current vs. gate voltage curves at elevated temperatures whereas the devices from other vendors show significant anomalous behavior indicating to mobile ion contamination either in the device or package. The strategies to address these issues include reduction of border traps and mobile ions by using a suitable oxidation process and reducing the operating gate voltage while keeping the gate oxide thickness fixed.

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