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Comparative Study of 6.5 kV 4H-SiC Discrete Packaged MOSFET, JBSFET, and Co-Pack (MOSFET and JBS Diode)

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***Abstract*— This paper reports the detailed comparison of packaged level, 6.5 kV rated 4H-SiC power MOSFET, MOSFET co-packaged with JBS diode (Co-Pack), and monolithically integrated 6.5 kV 4H-SiC MOSFET and JBS diode (JBSFET). JBSFET was designed to disable the PN turn for reliability purposes and save the chip and process cost from the one-chip integration and single metal scheme. Static and dynamic electrical characteristics of stand-alone MOSFET, Co-Pack, and JBSFET are compared to signify the benefit of JBSFET in terms of performance, reliability, and economical point of view.**

Keywords*— Silicon Carbide, 4H-SiC, MOSFET, JBSFET, Co-Package, Medium Voltage, Double Pulse Test (DPT), Switching, Short Circuit Capability, Stress, Body Diode Degradation

I. Introduction

Medium voltage (MV) power devices are utilized in DC-DC and synchronous buck converters for locomotives, military vehicles, and power grid converters, to name a few. Currently, MV power electronics are operated using >6.5 kV Si-IGBTs. The use of Si and bipolar currents in IGBTs suffers from large power loss and slow switching speed, limiting their use in high-frequency applications [1]. To overcome these issues, the development of energy-efficient 6.5 kV SiC-based power switches and their evaluation at the package level becomes extremely critical in enhancing next-generation power applications. The utilization of SiC also enables to downsize the volume and weight of the power system due to the superior material properties of SiC.

Discrete packaged MOSFETs are often externally paired (i.e. anti-parallel connection) with a Schottky diode in half-bridge and full-bridge converter configurations to avoid PN turn-on of the inherent body diode in the MOSFET during the freewheeling event at dead-time. However, medium voltage (3.3 kV - 20 kV) power MOSFETs typically require a larger size Schottky diode to prevent PN turn-on due to dominance of drift resistance (R_{drift}) [2].

It is important to disable the body diode as bipolar current reduces the switching speed and expands basal plane dislocations (BPDs) into stacking faults (SFs) that affect the current-voltage characteristic of the MOSFET [3]. In this aspect, a monolithically integrated MOSFET and JBS diode (JBSFET) is an attractive architecture for disabling body diode conduction and saving the chip area to reduce cost; critical for medium voltage (MV) SiC devices that rely on the expensive, thick epitaxial layer.

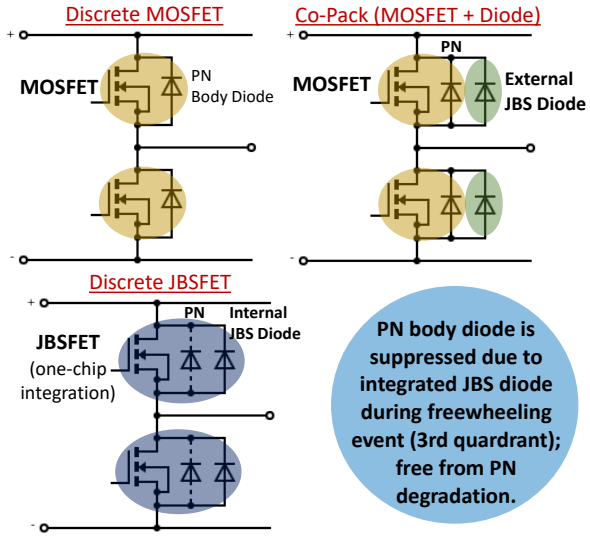

Fig. 1. Single-phase leg, half-bridge configuration of 4H-SiC MOSFETs, Co-Packs, and JBSFETs used in DC-DC and synchronous buck converters. The chip area is significantly reduced using single-chip, integrated JBSFET.

This paper presents the comparison of packaged devices such as 6.5 kV MOSFETs, JBS diodes, and JBSFETs that were fabricated at X-FAB, TX, USA. This work provides the first comprehensive evaluation and comparison of static and dynamic characteristics of discrete packaged MOSFET and JBSFET with co-packaged MOSFET and JBS diode (i.e. co-pack). In addition, packaged JBSFET and Co-Pack have undergone current stress to examine body diode degradation for reliability purposes.

II. Device Structure and Fabrication Technology

Fig. 1 shows a single-phase leg, half-bridge configuration using discrete packaged MOSFETs, Co-Packs (MOSFET + diode), and JBSFETs. Schematic cross-sectional images of fabricated 6.5kV 4H-SiC MOSFET, JBS diode, and JBSFET used in this study are shown in Fig. 2, respectively.

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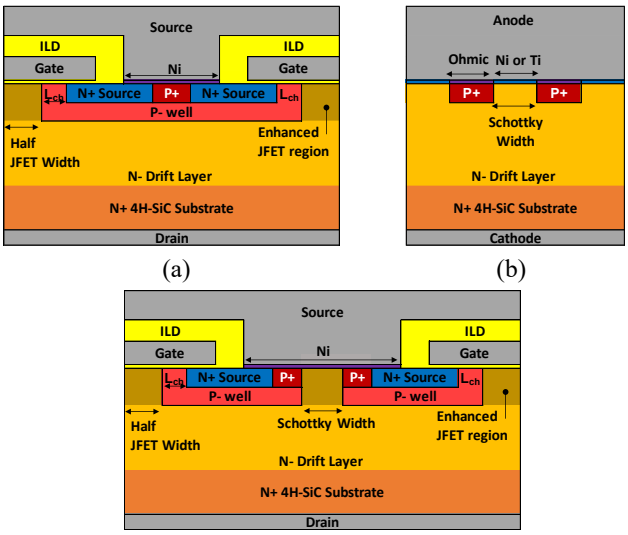


Fig. 2. Schematic cross-sectional image of fabricated 6.5kV 4H-SiC (a) MOSFET, (b) JBS diode, and (c) JBSFET.

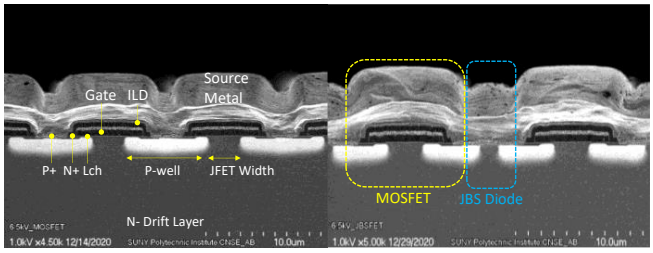


Fig. 3. Cross-sectional SEM image of (a) MOSFET and (b) JBSFET.

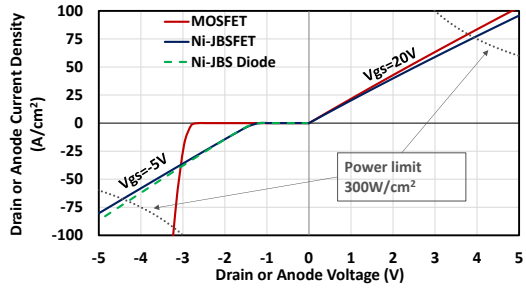


Fig. 4. Simulated results of MOSFET, JBS diode, and JBSFET at 25°C to highlight motivation of using JBSFET.

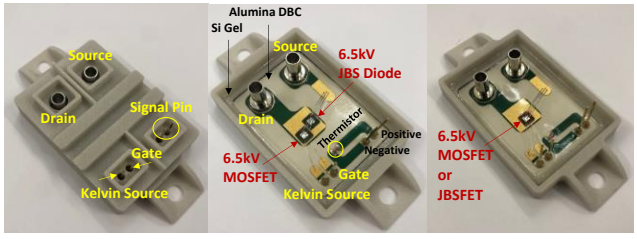


Fig. 5. Images of SUNY-designed MV power package: (a) external view, (b) internal view of a Co-Pack, and (c) internal view of a MOSFET or a JBSFET. Important parts are labeled.

In JBSFET, the P-well area was interrupted to allocate an opening for the Schottky contact (Fig. 2. (c)). Nickel (Ni) metal was used to form Schottky contact on the N-epi layer and ohmic contacts on N+ and P+ implanted area using a single annealing process, which dramatically simplifies the process scheme. This single metal, single annealing process at a specific temperature of 900°C is accompanied by an increased contact resistance that is detrimental to the on-resistance of low voltage (< 1.2 kV) SiC JBSFET. However, when it comes to 6.5 kV JBSFET, the increased contact resistance is diluted by the much larger resistance from the drift layer. Therefore, the proposed metal scheme becomes very attractive for 6.5 kV-rated 4H-SiC JBSFETs. In addition, without using this single process approach, the formation of two different metals for ohmic contacts and Schottky contacts would require a much more complicated process scheme. It is important to note that the same MOSFET process was used to fabricate Ni-JBSFET, saving an additional masking step.

In the best of the author's knowledge, this is the pioneer demonstration of 6.5 kV-rated 4H-SiC JBSFETs on 6-inch substrates at pure-play SiC/Si semiconductor fabrication foundry. Details of 6.5 kV MOSFET design and fabrication procedure of low voltage (600 V), Ni-JBSFET were previously reported in [4] and [5]. A cross-sectional SEM view of the fabricated 6.5 kV 4H-SiC MOSFET and JBSFET are shown in Fig. 3, respectively.

Sentaurus 2-D TCAD simulation results on pure MOSFET, JBS diode, and JBSFET at room temperature, in Fig. 4, illustrate the advantage of using JBSFET. The JBSFET operates in a unipolar mode during the 3rd quadrant characteristic, preventing basal-plane-dislocation (BPD) induced related degradation for long-term, reliable operation while sacrificing a small portion of on-resistance.

After the successful device fabrication, devices were packaged in a SUNY-designed MV power package. Fig. 5 depicts the external and internal view of MV custom packaging technology platform for discrete MOSFET and JBSFET, and Co-Pack (MOSFET + JBSFET) devices. All chips have the same active area of 4.5 mm^2.

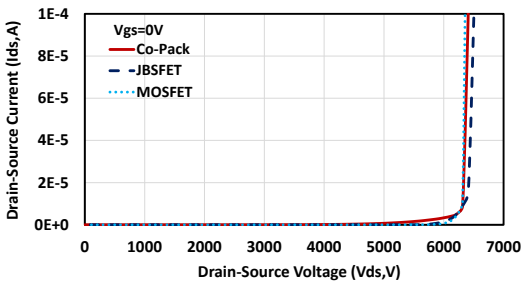
III. Experimental Results

A. Static Characteristics

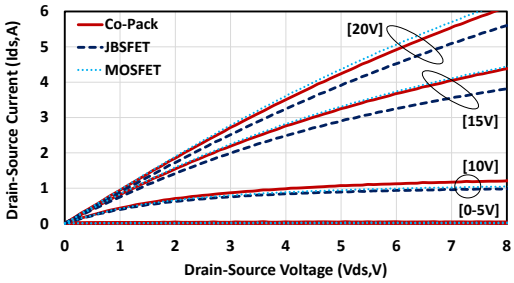
Fig. 6 compares the static characteristics (forward I-V, forward blocking, and 3rd quadrant operation) at 25 ºC of fabricated the packaged MOSFET, Co-Pack, and JBSFET.

Fig. 6 (a) shows that all three devices demonstrated a breakdown voltage of 6.5 kV at drain-source current (I_{ds}) of 100 µA. A combination of P+ rings and JTE-based edge termination, Hybrid-JTE, was used [6]. Forward current-voltage characteristic in Fig. 6 (b) exhibits that the on-resistance of the JBSFET is slightly higher than the MOSFET and Co-Pack due to the inclusion of the Schottky region in the unit-cell of the monolithically integrated SiC chip, increasing the cell pitch. Extracted specific on-resistance ($R_{on,sp}$) at a gate-source voltage (V_{gs}) of MOSET, Co-Pack, and JBSFET are 45 mΩ-cm^2, 45 mΩ-cm^2, and 47 mΩ-cm^2 at 25°C, respectively.

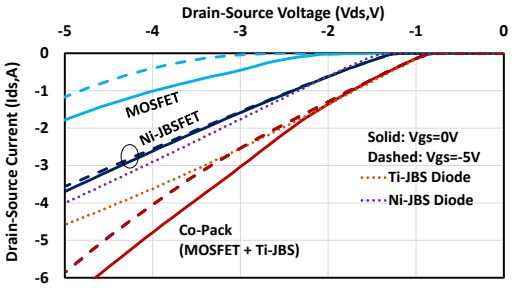
The JBSFET also exhibits a slightly higher knee voltage when operating in 3rd quadrant mode than the Co-Pack due to Ni Schottky metal, while the diode in Co-Pack has titanium



(a)



(b)



(c)

Fig. 6. Typical (a) blocking, (b) output, and (c) 3rd quadrant characteristics of discrete packaged MOSFET, JBSFET, and Co-Pack measured at 25°C.

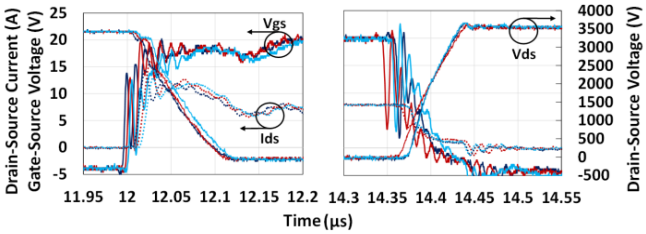


Fig. 7. Double pulse test using half-bridge configuration. Devices were tested at Rg = 10 Ω, Vds = 3.5 kV, Vgs = 20 V, and I_{load} = 6 A.

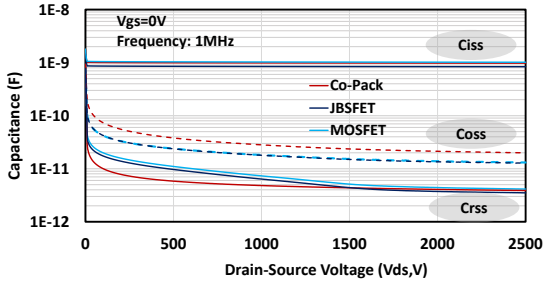


Fig. 8. Measured C_{iss}, C_{oss}, and C_{rss} at 1 MHz.

(Ti) Schottky (Fig. 6 (c)). Despite the high knee voltage from the JBSFET, JBSFET still offers a higher unipolar current conduction while the PN body diode of Co-Pack is activated at I_{ds} of ~ -2 A. This suggests that a larger size JBS diode is necessary to extract a higher current to suppress body diode conduction of the MOSFET in the Co-Pack configuration due to immense drift resistance in MV power semiconductor switches. It is important to note that unipolar operation in the freewheeling event (3rd quadrant mode) is imperative because the development of BPDs into SFs affects the device operation, which is critical for long-term reliability operation.

B. Double Pulse Test; Switching Speed

A double pulse test (DPT) was conducted using a half-bridge configuration on MOSFET, Co-Pack, and JBSFET as shown in Fig. 7. Devices were tested using gate resistor (R_g) of 10 Ω, drain-source voltage (V_{ds}) of 3.5 kV, V_{gs} of 20 V, and load current (I_{load}) of 6 A.

Extracted turn-on energy loss (E_{on}) of MOSFET, Co-Pack, and JBSFET from DPT is 1.54 mJ, 1.65 mJ, and 1.48 mJ, while turn-off energy loss (E_{off}) is 0.24 mJ, 0.29 mJ, and 0.18 mJ, respectively. The JBSFET demonstrated superior switching performance over Co-Pack, thanks to the one-chip integration of the Schottky area resulting in low capacitances as observed in Fig. 8 [7]. On the other hand, Co-Pack exhibits slightly larger E_{on} and E_{off} than the pure MOSFET due to additional anode-cathode capacitance (C_{ad}) from the anti-parallel diode being added to the MOSFET. This increases output capacitance ($C_{oss} = C_{ds} + C_{gd} + C_{ad}$).

C. Short Circuit Capability

Short circuit capability for all three devices were tested at V_{gs} of 20 V and V_{ds} of 3.5 kV. As observed in Fig. 9, MOSFET and Co-Pack demonstrated identical short circuit withstand time (SCWT) of ~ 6 µs while SCWT of JBSFET is ~ 5 µs. The lower SCWT of JBSFET compared to the MOSFET could be due to melted aluminum penetrating through the Schottky contact or high leakage current path from the Schottky barrier lowering [8]-[9].

D. Body Diode Degradation; Stress Test

JBSFET and Co-Pack were stressed at I_{ds} of -5A for 20 hours to evaluate body diode degradation for the device reliability purpose. V_{gs} of -5V was applied to ensure that the current path through the channel is fully closed.

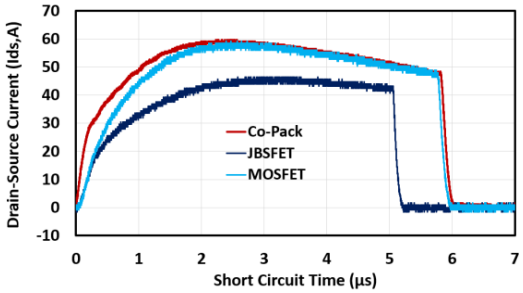


Fig. 9. Measured short circuit capabilities of MOSFET, Co-Pack, and JBSFET. Tested at V_{gs} of 20 V and V_{ds} of 3.5 kV.

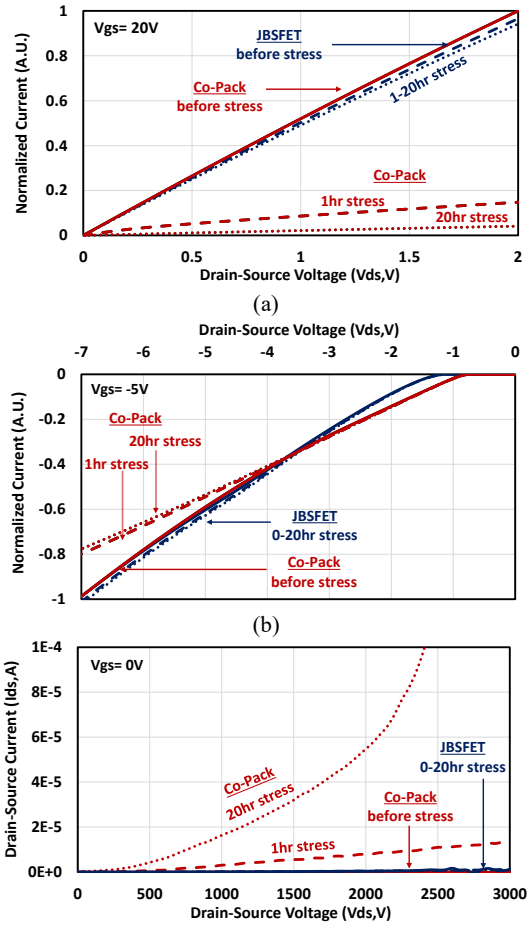


Fig. 10. Measured (a) I-V, (b) 3rd quadrant, and (c) breakdown voltage of JBSFET and Co-Pack before and after the stress. Devices were stressed at I_{ds} = -5 A and V_{gs} = -5 V.

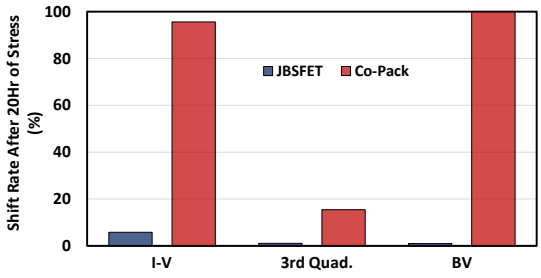


Fig. 11. Shift rate of JBSFET and Co-Pack after 20 hours of stress.

Fig. 10 depicts measured static characteristics of JBSFET and Co-Pack before and after 20 hours of stress. In terms of forward I-V, 3rd quadrant, and forward blocking mode, Co-Pack results in substantial degradation, while the JBSFET exhibits minimal changes. The rate of change for JBSFET and Co-Pack after 20 hours in Fig. 11 exhibits that the JBSFET approach provides reliable vehicle than the Co-Pack.

Table I summarizes the experimental results of fabricated 6.5 kV SiC MOSFET, Co-Pack, and JBSFET. Based on this study, it is concluded that JBSFET is the best approach from a reliability, economics, and performance point of view for current and future MV applications.

Table I
Summary of Experimental Results

	MOSFET	Co-Pack	JBSFET
Ron,sp (mΩ-cm^2)	45	45	47
BV (kV)	6.5		
Ciss (pF)	1017	979	837
Coss (pF)	13.1	19.9	12.7
Crss (pF)	4.13	3.88	3.52
Eon (mJ)	1.54	1.65	1.48
Eoff (mJ)	0.24	0.29	0.18
SC (µs)	6	5.8	5.1

*$R_{on,sp}$ at V_{gs} of 20V *BV at I_{ds} of 100µA
*Capacitances at V_{ds} of 2.5kV

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