

Body Diode Reliability of Commercial SiC Power MOSFETs

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Abstract— Stacking faults in the drift layer of 1.7 kV 4H-SiC MOSFETs result in body diode degradation, poor carrier conduction in on-state, and high leakage current in off-state. In this paper, the results of forward-bias stress on body diodes are analyzed in commercially available 1.7 kV 4H-SiC MOSFETs. Some devices show a significant degradation after forward-bias stress on the internal body diode. This implies that there are significant number of Basal Plane Dislocations (BPDs) present in these devices. These BPDs may be originally present in the drift layer or they may be induced by processing such as room temperature ion-implantation.

Keywords—Body diode, silicon carbide, MOSFET, basal plane dislocation, stacking fault

I. INTRODUCTION

In order to have a stable operation at high power densities and elevated temperatures, Silicon Carbide (SiC) MOSFETs, including JFETs, IGBTs, and thyristors, have greatly improved in wafer growth technology and device processing. Despite the major progress in SiC process technology, unipolar and bipolar SiC devices have yet to be fully implemented in higher voltage applications due to body diode degradation [1]-[5]. Basal plane dislocations (BPDs) in the drift layer of the device turn into stacking faults (SFs) which cause body diode degradation [6]. When the internal body diode is forward-biased, the electron-hole pairs recombine within the drift layer. This recombination provides the energy to activate the SFs. The carrier lifetime and mobility decrease due to the SFs. The effect of recombination-induced SFs on the majority carrier conduction current and the reverse leakage current in forward blocking mode after forward conduction stress on the body diode was first demonstrated in 2007 using the 10 kV SiC MOSFET [7]. Since the stacking fault size depends on the drift layer thickness, the body diode degradation is more problematic in high-voltage devices which need a thicker drift layer. The BPDs can originate from substrate [8], be formed during epi-layer growth [9], or be created during subsequent device fabrication processes [10]. Recently, Stahlbush *et al* reported that BPDs are also created by high dose Aluminum (Al) implantation process [11]. The main objective in this paper is to figure out how stacking faults affect majority carrier conduction and reverse leakage current in commercial 1700 V SiC MOSFETs from various vendors in Table I.

TABLE I. TESTED COMMERCIAL SiC POWER MOSFETs

Device	Gate Structure	Voltage Rating	Current Rating
Device D”	Trench	1700 V	3.5 A
Device E”	Planar	1700 V	5.0 A
Device G	Planar	1700 V	5.0 A

II. EXPERIMENTS

The following tests were performed on these devices. The 3rd quadrant I_D - V_D characteristics, 1st quadrant I_D - V_D and I_D - V_G characteristics, and forward leakage current in forward blocking mode were measured at room temperature. The I - V characteristics of the packaged devices were measured using a Keysight B1505A power device analyzer. To apply forward-bias stress on the body diode, 10 devices were connected in series where the body diodes were forward-biased as shown in Fig. 1. The DC power supply current was set at the appropriate device current rating. Isolated DC-DC converters and low-dropout regulators (LDOs) were used for each device to guarantee stable gate-source voltages during operation. To forward bias the body diode, a negative bias was applied to the drain with source grounded while a bias of -5 V was applied to the gate to ensure the complete pinch-off of the MOS channel. The body diode was stressed in forward conduction for 10 hours. Following this initial stress, all the measurements were repeated. After the stress, the devices were allowed to cool down to room temperature before the electrical measurements. This process was repeated after 20 hours and 100 hours. During the forward bias stress on the body diode, the devices were mounted on a heat sink with a water chiller to maintain a case temperature of the MOSFET package below 50°C.

III. RESULTS AND DISCUSSION

A. 3rd Quadrant Body Diode Characteristics

The 3rd quadrant I_D - V_D characteristics of the body diode are shown in Fig. 2 for devices from the vendors listed in Table I. The devices from all vendors show a built-in voltage of approximately -3 V with a gate voltage of -5 V. There was no current degradation in the body diode after forward stress on device E”. This indicates that the devices have been fabricated in sufficiently low BPD epitaxial layer or body diode has been somehow been prevented from getting forward biased.

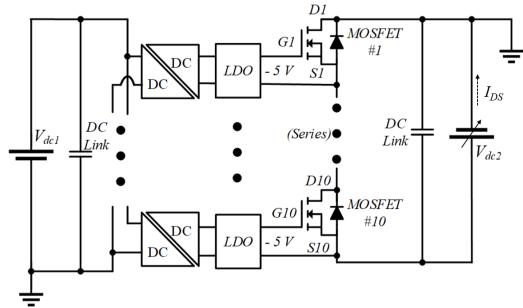


Fig. 1 Schematic of the body diode test circuit with ten (10) commercial SiC MOSFETs.

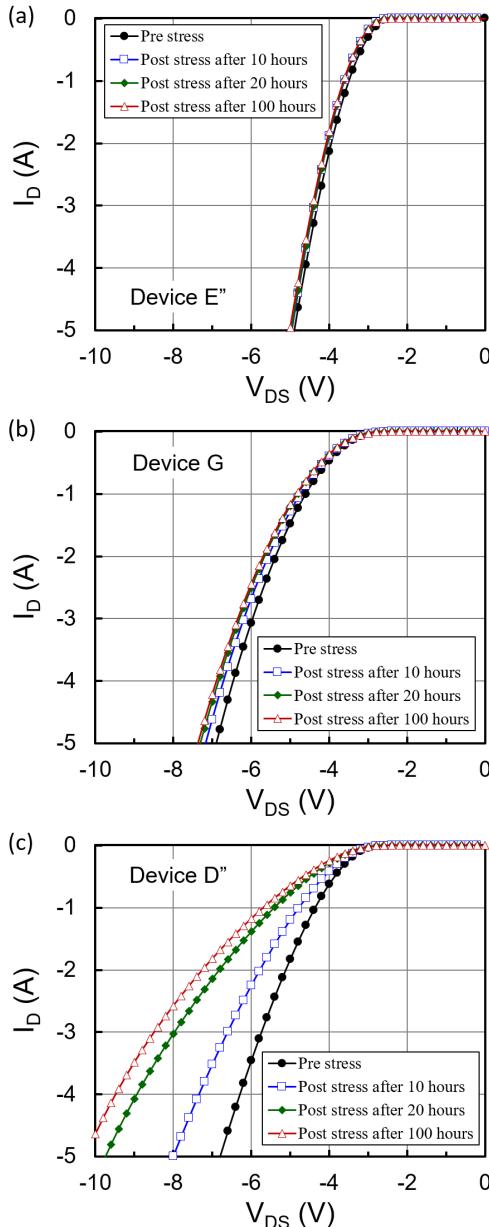


Fig. 2 Degradation of the 3rd quadrant I_D - V_D characteristics for built-in body diode of one selected 1.7 kV SiC DMOSFET from each vendor. The devices were stressed at 5 A (Device E'' and G) and 3.5 A (Device D'').

In the case of device G, two of the 10 devices show an increased forward voltage with increasing stress time. After 100 hours of forward bias stress, the forward voltage shift is found to be about 9% in device G. When the MOS channel is turned off and the body diode is forward biased, the holes in the p-well region are injected to the drift layer. The electron-hole recombination in the drift layer provides the energy to activate SFs. The recombination-induced SFs cause reduction of both the carrier lifetime and the mobility. Moreover, the spatial size of the SFs depends on the thickness of the drift layer. For example, the thickness of the drift layer of 1.7 kV 4H-SiC MOSFET is about 20 μm grown on a 4° off-axis substrate. Thus, the projection length of SF on the top surface will be about $20 \mu\text{m}/\tan 4^\circ = 286 \mu\text{m}$ [7]. All tested devices D'' were degraded after forward stress as shown in Fig. 2 (c).

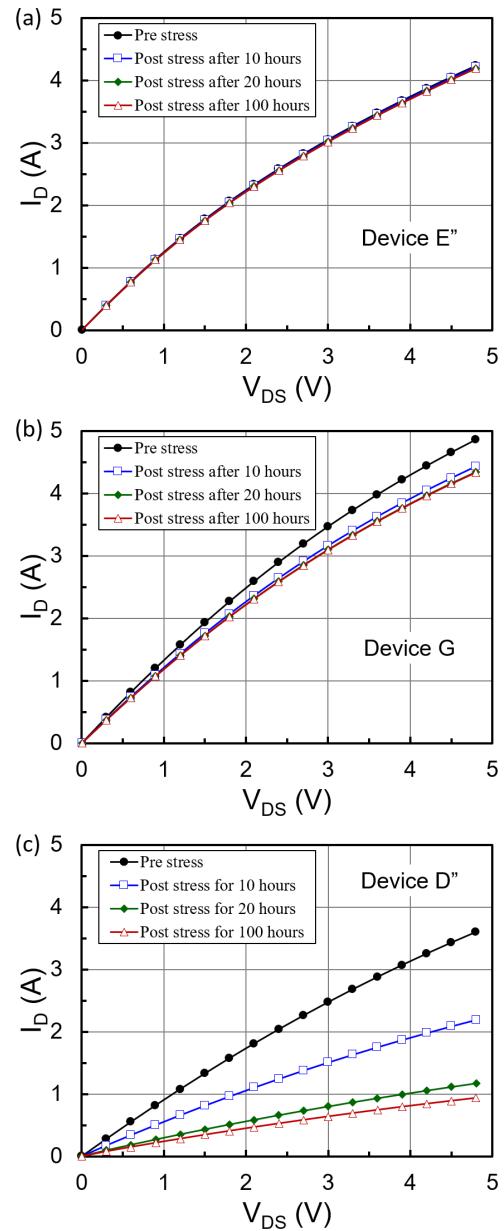


Fig. 3 Degradation of the 1st quadrant I_D - V_D characteristics at gate voltage $V_{GS} = 20$ V of one selected 1.7 kV SiC DMOSFET from each vendor. The curves are shown before and after stressing the body diode at 5 A (Device E'' and G) and 3.5 A (Device D'').

The forward voltage is checked at 3.5 A, which is the current rating of these devices. The forward voltage was measured as 6 V before the forward stress test. It increased to approximately 9 V after inducing forward stress for 100 hours. The forward voltage shift of the device D'' is found to be ~6 times higher than that of the device G. Therefore, these results imply one of four reasons may be responsible for such a high degree of degradation. First, that device D'' may be using room temperature ion implantation of Al to form p⁺ contacts which can create many BPDs. Second, some other process may result in the creation of BPDs. Third, the starting epi-layer has many BPDs. Lastly, BPDs can be introduced from the Al implanted region and glide through the epitaxial layer during the annealing [11].

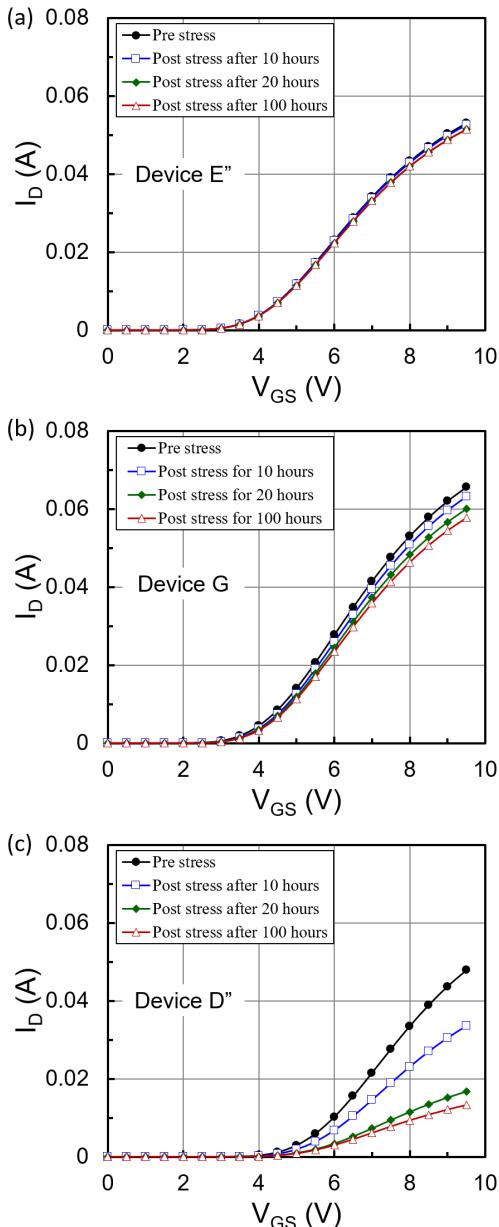


Fig. 4 Degradation of the 1st quadrant I_D - V_G characteristics at drain voltage $V_{DS} = 0.1$ V of one selected 1.7 kV SiC DMOSFET from each vendor. The curves are shown before and after stressing the body diode at 5 A (Device E'' and G) and 3.5 A (Device D'').

B. 1st Quadrant Output and Transfer Characteristics

The 1st quadrant I_D - V_D characteristics at the gate voltage of 20 V with forward stress times of 10 hours, 20 hours, and 100 hours are shown in Fig. 3. It shows that the on-resistance ($R_{ds,on}$) is increased in the devices that have body diode degradation. The $R_{ds,on}$ increase, which is completely dominated by the majority carrier conduction, is observed in device D'' and G since SFs not only act as recombination traps but also interrupt the flow of majority carriers [7]. Device D'' shows the greatest amount of the $R_{ds,on}$ increase (about 3.8 times) after 100 hours of stress among all tested devices showing that there are the highest number of SFs in the active area.

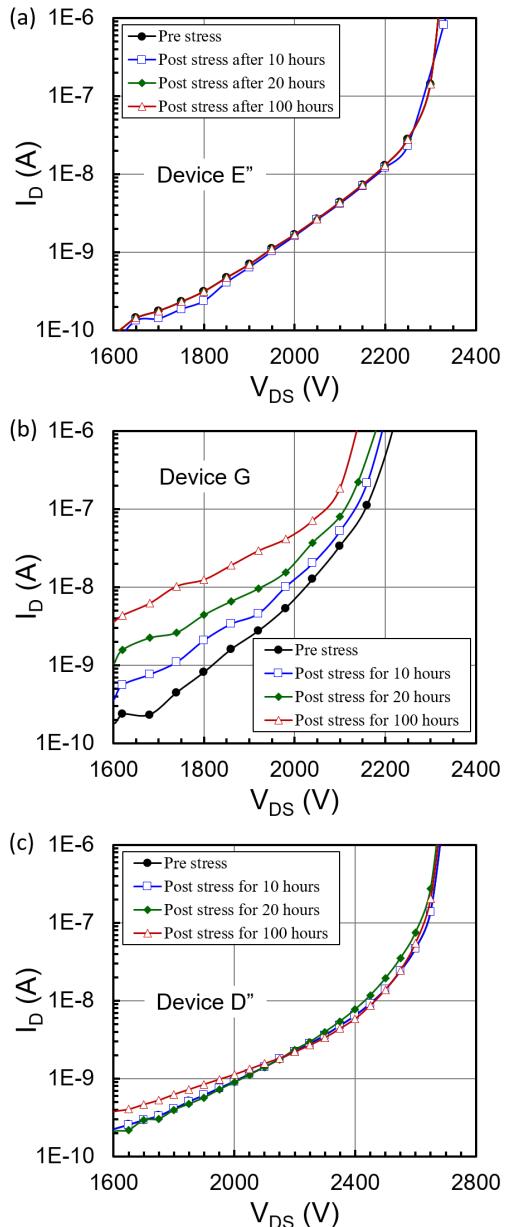


Fig. 5 Reverse bias characteristics at gate voltage of $V_{GS} = 0$ V of one selected 1.7 kV SiC DMOSFET from each vendor at room temperature before and after stress of the body diode at 5 A (Device E'' and G) and 3.5 A (Device D'').

The 1st quadrant I_D - V_G characteristics at the drain voltage of 0.1 V as a function of forward stress time are shown in Fig. 4. It is shown that the threshold voltage has not changed after stress on the body diode. Once again, drain current is degraded in the devices that have body diode degradation since SFs only affect the majority carrier conduction in the drift layer. In addition, it is clear from device D'' that almost all SFs are activated after 20 hours due to a sharp decrease in drain current. Beyond 20 hours, there is little change in drain current.

C. Forward Leakage Current in Forward Blocking Mode

The leakage current in forward blocking mode at room temperature before and after stress is shown in Fig. 5. The

forward leakage current has a gradual increase in device G with increasing stress on the body diode. Furthermore, the decrease in breakdown voltage is attributed to the increase in leakage current. Also, breakdown seems to happen in active area, caused by recombination-induced SFs. However, device D" and E" show no significant change in leakage current. Results from device E" are expected since this vendor might be using sufficiently low BPD epitaxial layer as discussed Section II-A. However, device D" does not show higher leakage current or reduced blocking after stress even though devices have a lot of SFs in active area. Therefore, it could be due to the fact that breakdown occurs in the edge termination region where there are no SFs.

These results have significant impact for the design and processing of SiC MOSFETs less than 1.7 kV. Some vendors may be using a heavy dose of Al implants at room temperature to form p⁺ contacts in the SiC MOSFETs. Although this process could reduce the device cost, it creates new BPDs [9]. If SiC MOSFETs are used without separate freewheeling diode chips in high frequency switching applications, the body diode will conduct during some portion of the switching cycle. Alternatively, SiC MOSFETs with built-in Schottky diodes are an alternative approach to reducing body diode degradation [12]. In addition, using separate freewheeling diode chips or blocking injection of minority carriers in the drift layer are good solutions.

IV. CONCLUSION

This paper has investigated the effects of body diode degradation in commercially available 1.7 kV SiC MOSFETs from various vendors. The already existing or process-induced BPDs turn into SFs after forward bias stress which results in significant body diode degradation. Only one vendor (E") did not show any degradation on ten devices after 100 hrs of stress. The other two vendors showed varying degrees of degradation. Using an external Schottky diode or built-in Schottky diode in the main MOSFET could be utilized for preventing the body diode degradation in SiC MOSFETs.

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