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A Static, Switching, Short-circuit Characteristics of 1.2 kV 4H-SiC MOSFETs: Comparison between Linear and (Bridged) Hexagonal Topology

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Abstract— This paper reports the layout approaches and resulting static, dynamic, and short-circuit (SC) ruggedness characteristics of 1.2 kV power MOSFETs fabricated on a 6-inch 4H-SiC substrate. Different layout topologies (linear and hexagonal) and different design variations (with and without bridge of P-well) were investigated to study their effect. It was experimentally demonstrated that 1) the hexagonal layout topology enables a low specific on-resistance ($R_{on.sp}$), 2) the linear MOSFET can be utilized in high frequency applications due to fast switching speed, and 3) the hexagonal topology with bridge offers greater reliability and ruggedness.

Keywords— Short-circuit ruggedness, Topology, Hexagonal, Linear, Switching, 4H-SiC, MOSFETs

I. Introduction

1.2 kV SiC MOSFETs are becoming more widely used in power electronics across various applications due to superior characteristics over conventionally employed Si IGBTs of similar rating. Depending on the specific application, the importance of various requirements, from a power semiconductor device perspective, are different. For example, low specific on-resistance is preferable to reduce conduction losses in electric vehicles (EV) [1]. High frequency applications need fast switching characteristics [2] to minimize switching losses. Aerospace and industrial applications require highly reliable and rugged devices [3]. In regards to the device architecture and process, many groups have been developing methods to improve conduction behavior [4], dynamic characteristics [5], and ruggedness [6]. However, detailed research regarding the layout approach, such as topology investigation of 1.2 kV 4H-SiC MOSFETs, is lacking; despite the specific attributes of a given power MOSFET topology fundamentally factoring into how the device performs. Consequently, it is of extreme interest to investigate SiC power MOSFET layout topology variations to understand which topologies are best suited for which applications.

In this paper, different layout topologies (linear and hexagonal) and different design variations (with and without bridge of P-well) are compared using the same mask set and process baseline to then propose a suitable SiC power MOSFET type for each application of interest. The comparison between different devices was performed in terms of the statics, dynamic switching, and short-circuit characteristics.

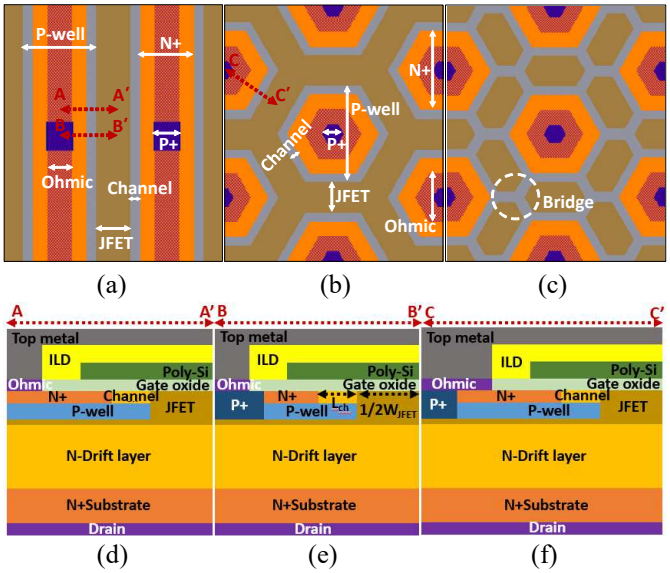


Fig. 1. Layout of (a) Linear MOSFET, (b) HEXFET, (c) B- (Bridged) HEXFET, cross-sectional view of (d) A-A', (e) B-B', (f) C-C'.

II. Device Design

Fig. 1 shows layout and cross-sectional views of the 1.2 kV SiC MOSFETs with different topologies, each having channel length (L_{ch}) of 0.4 µm and half JFET width ($1/2W_{JFET}$) of 0.7 µm. Accumulation-mode channel MOSFETs were designed to obtain higher channel mobility. In order to minimize JFET resistance, JFET implantation with current spreading layer (CSL) was adopted in the fabricated MOSFETs. P+ source is placed in the orthogonal direction to reduce the cell pitch in MOSFET with the linear topology as shown in Fig. 1 (a). Fig. 1 (d) and (e) pertain to the MOSFET with orthogonal P+ sources and show the cross-sectional views of portions that include N+ source contact and P+ source contact, respectively. However, the cell pitch of MOSFETs with hexagonal topology

increases due to the inclusion of P+ source as shown in Fig. 1 (b), (c), and (f). Although hexagonal topology has wider cell pitch, the high conduction behavior can be maintained due to the higher channel density. P-well bridge structure was added to protect the corner of hexagonal p-well from high electric-field concentrations (B-HEXFET, Fig. 1(c)).

III. Device Fabrication Technology

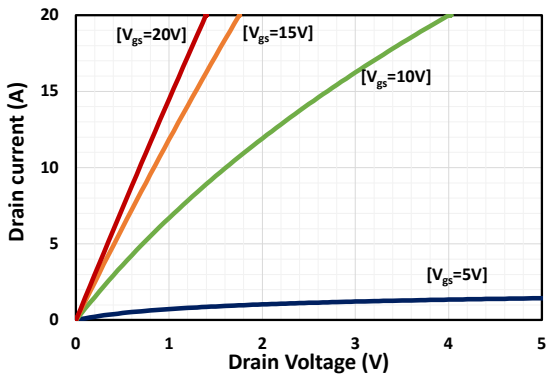
The devices were fabricated by Analog Devices, Inc. (ADI) fabrication facility in Hillview, San Jose, CA, using the same base process line described in [7]. A 10 µm thick drift layer with N- type doping concentration of 8×10^{15} cm^{-3} on 6-inch, N+ 4H-SiC substrate was used for the fabrication of 1.2 kV MOSFETs. Aluminum and Nitrogen ion implants were used to form P-well/P+ source/JTE, and JFET region/N+ source, respectively. After all implantation steps done, a 1650 °C, 10-min activation anneal with a carbon cap was conducted. A 50 nm thick gate oxide was formed by a combination of ultrathin (2 nm) thermal oxide and 48 nm of deposited oxide, followed by a post oxidation anneal (POA) in N_2O ambient. The N-type polysilicon was deposited and patterned for the formation of the gate. After, undoped silicon glass (USG) was deposited as interlayer dielectric (ILD), then patterned and etched to make ohmic contact regions. Nickel (Ni) was deposited on the frontside, followed by an RTA for the silicidation process. Next, unsilicided Ni metals were removed and annealed by RTA at 965 °C for 2 minutes. Backside was then deposited with Ni, followed by the same RTA process. A 4 µm thick Ti/TiN/Al stack was deposited for the source and gate metal. Silicon nitride and polyimide were used for the passivation. Finally, a solderable metal stack was deposited on the backside.

IV. Results

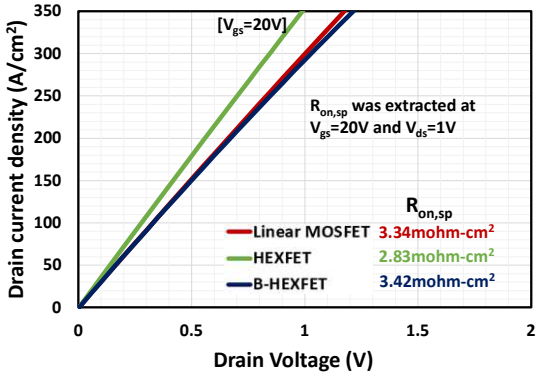
A. Statics Characteristics

Fig. 2 (a) shows output characteristics of 1200 V/~30 A HEXFET. The measurement was conducted at gate biases of 5 to 20 V with 5 V steps. The high conduction behaviors were achieved thanks to expertly optimized cell structure and process. The JFET region was optimized using the enhanced JFET doping with current spreading layer (CSL). Moreover, by using accumulation mode channel, the channel resistance was minimized. Fig. 2 (b) compares the output characteristics of the different topologies (note: substrate thinning process was not employed). $R_{on,sp}$ was extracted at V_{gs} of 20 V and V_{ds} of 1 V. As noticed, HEXFET offers the lowest $R_{on,sp}$ due to higher channel density as summarized in Table I. Since the P-well bridge reduces the current path in the JFET area, $R_{on,sp}$ is higher in case of B-HEXFET.

Transfer characteristics and transconductance are shown in Fig. 3 (a). Transfer characteristics was measured at V_{ds} of 0.1 V. Regardless of topologies and designs, threshold voltages (V_{th}) are identical (2.3 V), but hexagonal topology provides low maximum transconductance (G_m) because the channel

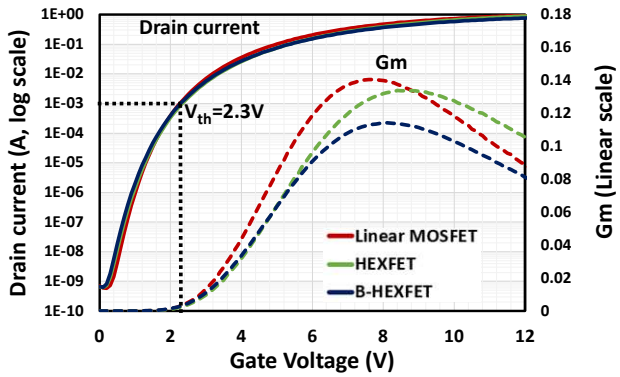


(a)

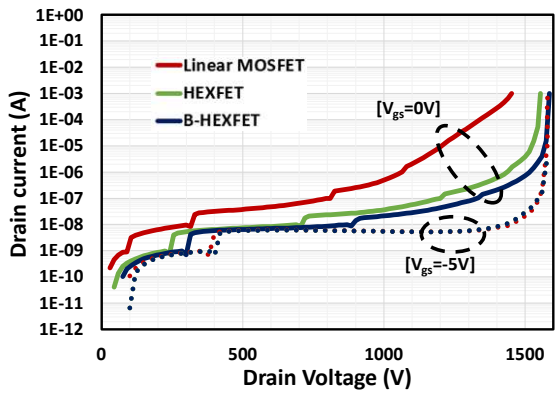


(b)

Fig. 2. Output characteristics of (a) HEXFET and (b) all devices. $R_{on,sp}$ was extracted at V_{gs} of 20 V and V_{ds} of 1 V.



(a)



(b)

Fig. 3. (a) Transfer characteristics, and (b) blocking behaviors of fabricated devices. V_{th} was extracted at V_{ds}=0.1 V and I_{ds}= 1 mA.

conductance for hexagonal structures is lower when compared with linear MOSFETs at the same gate voltage. Especially, B-HEXFET has the lowest channel conductance, resulting in the lowest G_m.

Fig. 3 (b) shows the blocking characteristics of the fabricated devices. In order to look into the cause of leakage current, different gate voltages were applied under the blocking mode of operation. At V_{gs} of -5 V, regardless of the split, high breakdown voltages with low leakage currents were achieved thanks to the efficient edge termination technique (Hybrid-JTE). When negative gate voltage is applied, the channel is closed, which contributes to the formation of high channel potential. The maintained channel potential under high drain voltage suppresses the leakage currents for all devices, especially the linear MOSFET. On the other hand, the leakage current increases at V_{gs} of 0V. In other words, leakage current stems from the channel under blocking mode at V_{gs} of 0 V. HEXFET and B-HEXFET provide high breakdown voltage at V_{gs} of 0 V with low leakage until breakdown, where the channel is effectively shielded by the hexagonal topology of P-well. Although hexagonal topology has higher channel density, the increased channel potential due to the surrounding P-well results in the reduction of the leakage current from the channel. Especially, B-HEXFET has lower leakage current because the bridge of the P-well improves the shielding effect.

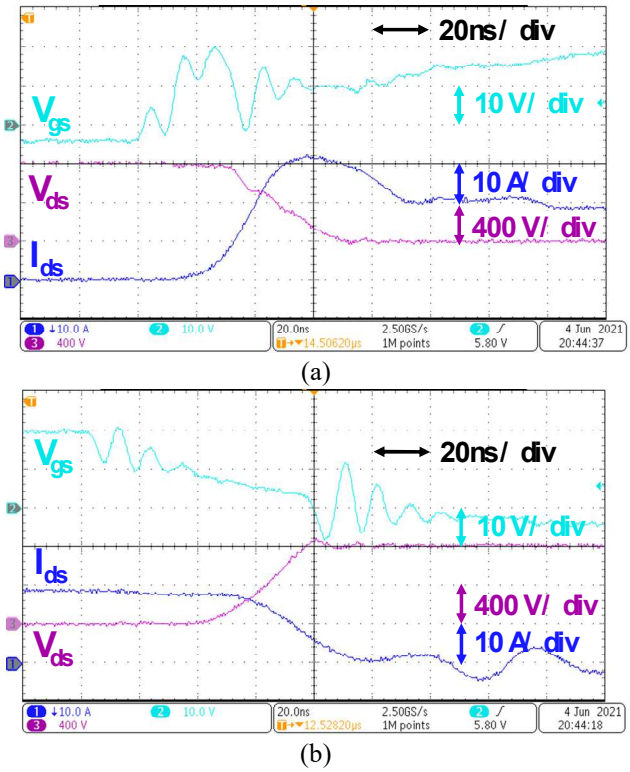


Fig. 4. Switching waveforms of linear MOSFET: (a) turn-on (b) turn-off at V_{gs}=-4/20 V (R_g = 20 Ω) and V_{ds}=800 V. **Switching speeds**: $t_{sw(on)}$ = 62.4 ns, $t_{sw(off)}$ = 74.7 ns, **Switching dv/dt**: switching on= 21.1 kV/µs, switching off= 24.3 kV/µs, **Switching losses** (V_{dc} = 800 V, I_{ds}= 18A): $E_{sw(on)}$ = 333 µJ, $E_{sw(off)}$ = 206 µJ.

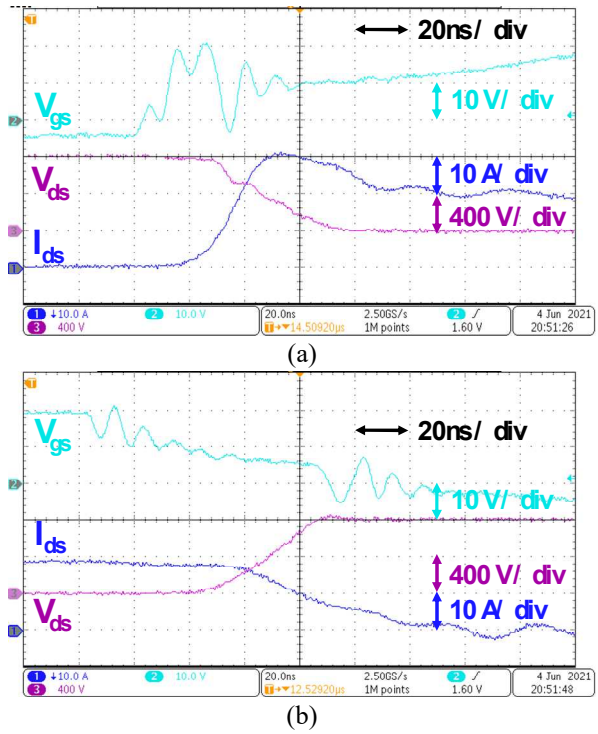


Fig. 5. Switching waveforms of HEXFET: (a) turn-on (b) turn-off at V_{gs}=-4/20 V (R_g = 20 Ω) and V_{ds}=800 V. **Switching speeds**: $t_{sw(on)}$ = 63.2 ns, $t_{sw(off)}$ = 78.6 ns, **Switching dv / dt**: switching on= 17.1 kV/µs, switching off= 19.0 kV/µs, **Switching losses** (V_{dc} = 800 V, I_{ds}= 18A): $E_{sw(on)}$ = 378 µJ, $E_{sw(off)}$ = 276 µJ.

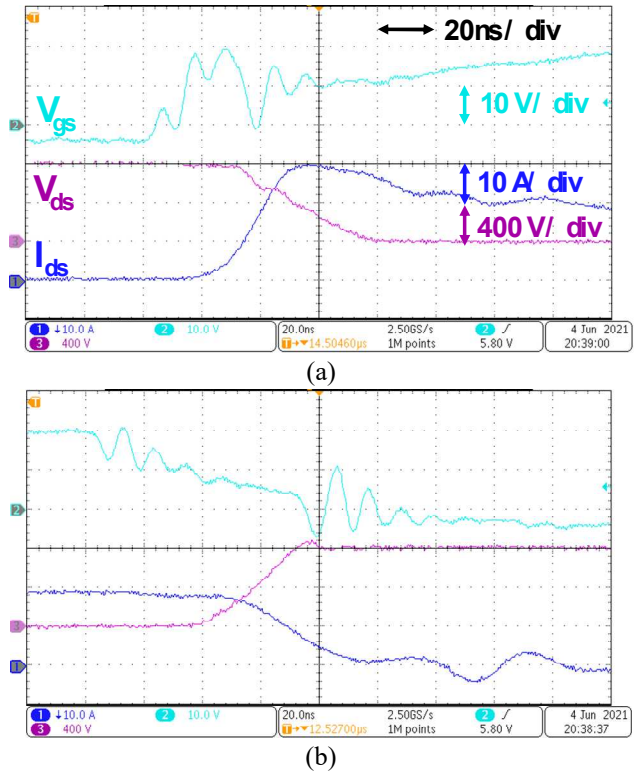


Fig. 6. Switching waveforms of B-HEXFET: (a) turn-on (b) turn-off at V_{gs}=-4/20 V (R_g = 20 Ω) and V_{ds}=800 V. **Switching speeds**: $t_{sw(on)}$ = 58.8 ns, $t_{sw(off)}$ = 63.5 ns, **Switching dv/dt**: switching on= 17.2 kV/µs, switching off= 25.0 kV/µs, **Switching losses** (V_{dc} = 800 V, I_{ds}= 18A): $E_{sw(on)}$ = 401 µJ, $E_{sw(off)}$ = 258 µJ.

B. Switching Characteristics

Fig. 4, 5, and 6 show the measured switching waveforms of turn-on and turn-off for linear MOSFET, HEXFET, and B-HEXFET, respectively. A double pulse test was used to evaluate switching characteristics of the devices. A DC supply voltage of 800 V was applied. The off/on gate voltage is -4/20 V, respectively, with R_g of 20 Ω used for the switching test. The switching energies for turn-on and turn-off are calculated at 10% V_{gs} to 10% V_{ds} and 90% V_{gs} to 90% V_{ds}, respectively. The switching results for all devices are summarized in Table I. Linear MOSFET has fastest switching behaviors for turn-on and turn-off. This is because linear MOSFET has low gate-drain capacitance (C_{rss}) [8] and high transconductance. HEXFET has high $E_{sw(off)}$ when compared with B-HEXFET in spite of low $R_{on,sp}$. The removal of P-well bridge causes the increase of JFET region, resulting in high C_{rss}.

C. Short-circuit Characteristics

Fig. 7 shows short-circuit (SC) waveforms of B-HEXFET. The SC condition is R_g of 20 Ω, V_{gs} of 20 V, and V_{ds} of 800 V. At the beginning of the SC test, maximum drain current occurs, contributing to the increase of junction temperature. Next, drain current starts decreasing because of the reduction in electron mobility at high temperatures.

Fig. 8 (a) shows drain current density of B-HEXFET with different gate pulse widths. In order to obtain short-circuit withstand time (SCWT, t_{sc}), the gate pulse width increases by 0.1 µs until the devices were failed. SCWT of 1.4 µs was achieved in B-HEXFET. Although the device endured a gate pulse width of 1.5 µs, B-HEXFET failed after the completion of the SC condition. This is due to the junction temperature decreasing much more slowly in the device than the SC drain current. Therefore, the DUT was continuously exposed to detrimental high temperatures, ultimately resulting in the degradation and failure of the device.

Fig. 8 (b) compares drain current density of all devices when the device is failure under SC event. The lowest maximum current density (J_{peak}), contributing to the reduction in the junction temperature was accomplished in B-HEXFET. A low J_{peak} results in the increase of t_{sc}, as the bridge of the P- well in the JFET region suppresses the current during SC conditions.

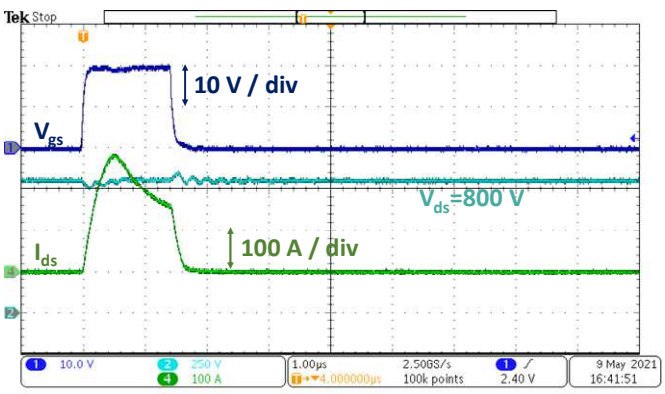
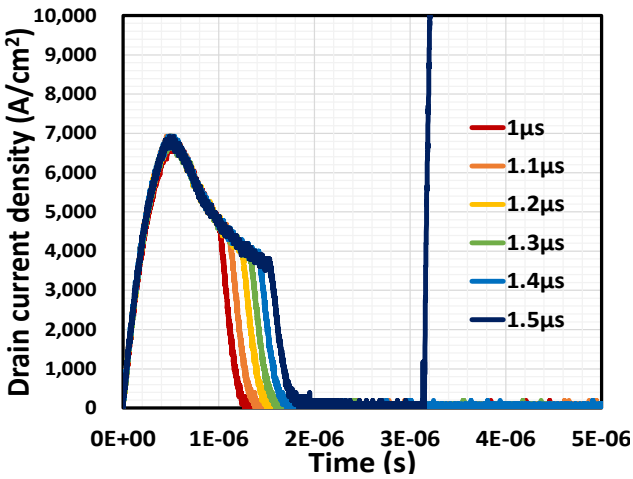
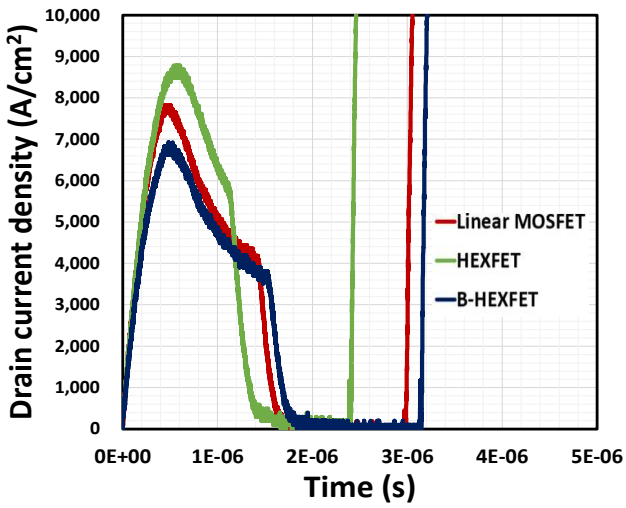


Fig. 7. Short-circuit robustness waveforms of B-HEXFET under V_{gs}=20 V and V_{ds}=800 V.



(a)



(b)

Fig. 8. (a) Drain current density of B-HEXFET with different gate pulse widths under short-circuit condition at V_{gs}=20 V and V_{ds}=800 V. (b) Drain current density of all devices when the device is failure under the short-circuit condition. For linear MOSFET, HEXFET, and B- HEXFET, SCWT (maximum current density) of 1.3 µs (7822 A/cm^2), 1.0 µs (8487 A/cm^2), and 1.4 µs (6830 A/cm^2) was achieved.

Although HEXFET provides good shielding effects under blocking characteristics, the highest maximum drain current density occurs under SC event, resulting in the shortest SCWT. This is due to the significantly reduced $R_{on,sp}$.

Table I summarizes design information and experimental results for linear MOSFET, HEXFET, and B-HEXFET. In order to compare the different topologies and designs, the cell pitch and the portion of cell were examined. The typical static characteristics, switching test, and short-circuit ruggedness were investigated to fairly compare the different layouts. HEXFET offers the lowest $R_{on,sp}$ with low leakage current, providing high breakdown voltage, which can be used in power electronics that require high efficiency performance. In high frequency applications, linear MOSFET can be utilized due to the low switching losses for both of turn-on and turn-off. For critical applications that require extreme ruggedness, hexagonal topology with bridge of P-well is favorable, since B-HEXFET provides better shielding effect, resulting in the improved reliability and robustness.

TABLE I
SUMMARY OF DESIGN INFORMATION AND EXPERIMENTAL RESULTS.

	MOSFET	HEXFET	B-HEXFET
Cell pitch (μm)	4.4	5.9	5.9
Channel area (%)	32	35	29
$R_{on,sp}$ [mΩ-cm^2] @ V_{gs}=20 V and V_{ds}=1 V	3.34	2.83	3.42
V_{th} [V] @ I_{ds}=1 mA	2.3	2.3	2.3
$G_{m(max)}$ [S]	0.14	0.134	0.114
BV [V] @ V_{gs}=0 V	1452	1554	1586
Leakage current [μA] @ V_{gs}=0V, V_{ds}=1200 V	9	0.1	0.04
$t_{sw(on)}$ [μs] @ V_{gs}=-4/20 V and V_{ds}=800 V	62.4	63.2	58.8
$t_{sw(off)}$ [μs] @ V_{gs}=-4/20 V and V_{ds}=800 V	74.7	78.6	63.5
Switching dv/dt (on) [kV/μs]	21.1	17.1	17.2
Switching dv/dt (off) [kV/μs]	24.3	19.0	25.0
$E_{sw(on)}$ [μJ] @ V_{gs}=-4/20 V and V_{ds}=800 V	333	378	401
$E_{sw(off)}$ [μJ] @ V_{gs}=-4/20 V and V_{ds}=800 V	206	276	258
J_{peak} (A/cm^2) @ V_{gs}=20 V and V_{ds}=800 V	7822	8487	6830
t_{sc} (μs) @ V_{gs}=20 V and V_{ds}=800 V	1.3	1	1.4

V. CONCLUSIONS

1.2kV 4H-SiC MOSFETs with different layout topologies (linear and hexagonal) and different design variations (with and without bridge of P-well) were investigated to study their effect on the static conduction, dynamic switching, and short-circuit characteristics. HEXFET provides the lowest $R_{on,sp}$ with high breakdown voltage due to the high channel area. Linear MOSFET has fast switching speed because of the low C_{rss} and high G_m. P-well bridge allows B-HEXFET to be more reliable and rugged thanks to shielding effect. Experimental measurements demonstrate which topologies are best suited for which power electronics applications.

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