3300-V SiC MOSFET Short-Circuit Reliability and Protection

Diang Xing, Xintong Lyu, Jiawei Liu, Chen Xie, Anant Agarwal, and Jin Wang
Center for High Performance Power Electronics (CHPPE)
The Ohio State University
Columbus, OH, USA
xing.174@osu.edu, wang.1248@osu.edu

2021 IEEE Applied Power Electronics Conference and Exposition (APEC) | 978-1-7281-8949-9/21/$31.00 ©2021 IEEE | DOI: 10.1109/APEC42165.2021.9487116

***Abstract*— This paper investigates the short-circuit (SC) capability of the 3.3-kV 5-A silicon carbide (SiC) metal–oxide–semiconductor field-effect transistor (MOSFET) from GeneSiC (Generation-1, engineering sample). The SC withstand time (SCWT) of the tested 3.3-kV device could not reach the benchmark of 10-µs at a 2.2-kV bus voltage and 18-V gate voltage. A three-step ultra-fast SC protection method is introduced and validated. It can detect a SC fault and reduce the saturation current within 80 ns, then softly turn off the device within 2 µs. Using this protection method, the SC energy can be reduced by around 32%. Additionally, a noise immunity test showed this protection would not be falsely triggered at the device's rated current. Medium-voltage (MV) SiC MOSFET based power conversion systems could utilize this method to enhance their SC capabilities without incurring efficiency losses.**

Keywords*— *Medium-voltage (MV), Silicon carbide (SiC), Metal–oxide–semiconductor field-effect transistor (MOSFET), Short-circuit (SC), SC protection

I. Introduction

Medium-voltage (MV) semiconductor devices have shown great potential for use in solid-state relays, traction inverters, and distribution grid converters [1]-[4]. Benefitted from the absence of tail currents and the decrease of reverse recovery times, MV silicon carbide metal–oxide–semiconductor field-effect transistors (SiC MOSFETs) can demonstrate higher switching speeds with lower switching losses compared to silicon insulated-gate bipolar transistors (Si IGBTs), yielding improved system performance [5]. However, compared with their Si counterparts, SiC MOSFETs have shorter channel lengths, thinner gate oxides, and higher saturation currents for the same die size, which result in worse short-circuit (SC) capability. Reported SC withstand times (SCWTs) of four different designs of 3.3-kV SiC discrete MOSFETs, denoted as A, B, C [6], and D [7], are summarized in Fig. 1. According to Fig. 1, all listed SiC devices could not survive 10 µs in SC events, even at less than 50% of their rated drain-source voltage, whereas Si IGBTs are designed according to the benchmark of 10-µs SCWT [8]. Additionally, SC-induced degradation of SiC MOSFETs electrical characteristics including increased on-resistance, threshold voltage shifts, and increased drain-source or gate-source leakage currents have been reported [9]-[11]. The poor SC ruggedness of SiC MOSFETs increases the risk of failures and limits their lifetimes in applications. The traditional MOSFET SC protection, based on the IGBT desaturation (DESAT) protection, has shown incapability to satisfy both

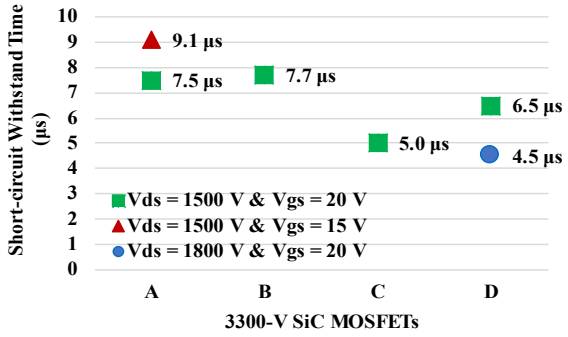


Fig. 1 Reported 3.3-kV SiC MOSFETs' SCWTs.

nanosecond-level response times and high detection accuracies.

During SC events, the device enters the saturation region, undergoing simultaneous high current and high voltage. Extremely high SC energy is generated within hundreds of nanoseconds which cannot be dissipated by the baseplate and the cooling structure, causing die temperatures rising outside of the safe operating zone. Lowering the saturation current when a SC fault happens is becoming one of the most promising approaches to improve the SC reliability of SiC devices. Some design methods to accomplish this include 1) P+ shielded MOSFET [12], 2) embedded source resistance MOSFET [13], 3) the Baliga SC Improvement Concept (BaSIC) [14], and 4) the three-step ultra-fast SC protection method [15], [16], etc. The P+ shielded MOSFET design implants a very high P-type doping concentration at the bottom of the P-well to shield the junction between the channel and JFET regions. Both channel length modulation (CLM) and drain-induced barrier lowering (DIBL) effects at short-channel devices can be alleviated, and the saturation current will not rise significantly with the drain-source voltage increasing. The fabrication time and cost for very high dose of P-type implantation are the major issues with this method. The embedded source resistance MOSFET design injects a positive temperature coefficient (PTC) metal between the N+ source ohmic contact and the top source metal. When a high positive drain-source current is flowing through the source metal resistance, the voltage drop can raise the voltage potential of the inversion layer. Thus, the voltage between the gate and N+ source is reduced, and the saturation current will be clamped to a lower level. However, this source resistance results in additional conduction losses under normal operation. The BaSIC method applies a nonlinear element with much lower on-resistance and smaller saturation current in series with the main

SiC MOSFETs. During a SC time, this nonlinear element will clamp the current to its saturation level. Compared with the embedded source resistance MOSFET, the BaSIC sacrifices less conductance performance, but the nonlinear element may increase the complexity of the main power loop circuit. The three-step ultra-fast SC protection method consists of nanosecond-level SC detection, active gate voltage clamping to reduce the saturation current, and DESAT-based protection. This protection circuit is integrated in the gate drive circuit and will not cause additional efficiency losses in the main power loop circuit. Previously, the three-step ultra-fast SC protection method has been experimentally verified with the 650-V gallium nitride (GaN) high-electron-mobility transistor (HEMT) [15] and the 600-V GaN gate injection transistor (GIT) [16], but not yet in SiC or MV devices.

In this paper, test results and saturation current measurements of the 3.3-kV SiC device at a 2200-V dc bus are presented in Section II. Section III introduces the classic three-step ultra-fast SC protection and extends it with two more modified versions. In Section IV, the protection function validation with the 3.3-kV SiC device is presented. A conclusion is given in Section V. The devices under test (DUTs) are 3.3-kV 5-A rated GeneSiC Generation-1 SiC MOSFET engineering samples. There are two different device samples (denoted as DUT #1 and DUT #2) used for SCWT measurement and SC protection tests respectively.

II. The SCWT of the 3.3-kV SiC MOSFET

The SC sustaining capability of DUT #1 is presented in this section. Before the destructive SC test, the I-V characteristics of DUT #1 were measured under both high drain bias and low drain bias with different gate voltages to explore the gate voltage's impact on SC energy and normal turn-on resistance.

Fig. 2 shows the SC test circuit where DUT #1 is directly connected with the capacitor bank. Two 5-μF film dc-link capacitors are utilized to realize an acceptable dc bus voltage dip during a SC event. Five 15-nF decoupling capacitors with a low equivalent serial inductance (ESL) and resistance (ESR) are placed near DUT #1 to support the high-frequency SC current. The external gate resistor is 20 Ω to ensure a slow turn-off. Current limiting resistors are placed between the power supply and the capacitor bank to decouple the power supply from the test setup during SC events. Bleeding resistors are added to ensure the test setup can shut down safely. The SC current was extracted by the voltage drop on a 0.1-Ω shunt resistor using a high bandwidth passive probe.

The SCWT of DUT #1 was measured with a 2.2-kV dc bus voltage at room temperature. The turn-on gate voltage was 18-V along with a 0-V turn-off gate voltage. The turn-on pulse width began at 1-μs, and a 1-μs increment was added for the next pulse until the device failed. Between two adjacent pulses, a minute interval was allowed for the device to cool down.

Fig. 3 shows the SC test waveforms when the DUT survived the 4-μs SC pulse and when the DUT failed at the 5-μs SC pulse. 0.9-J energy was generated within the 5-μs SC pulse, which caused the semiconductor die to reach its critical temperature. The saturation current initially rose due to the increase of effective inversion layer electron mobility with temperature, and

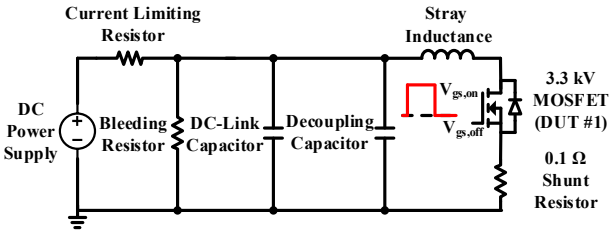
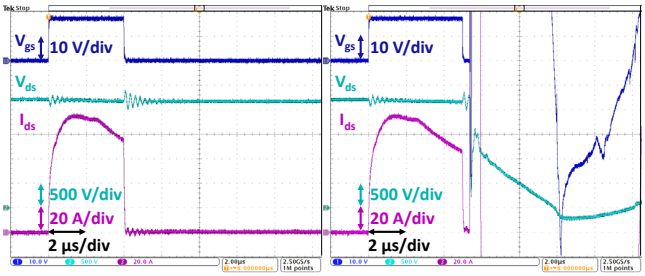


Fig. 2 SC test circuit for the 3.3-kV SiC MOSFET.



(a) (b)

Fig. 3 The SC tests waveforms: (a) DUT #1 survived at the 4-μs pulse; (b) DUT #1 failed at the 5-μs pulse after switching off.

then the current was reduced due to the net reduction in the inversion layer and drift layer electron mobilities at higher temperature [17], [18]. DUT #1 failed catastrophically after the gate voltage reduced to 0 V, which could be caused by the molten aluminum diffusing to the depletion region [19] or thermal runaway at hot spots [20]. The SC currents from the first to the fifth turn-on pulse are plotted in Fig. 4, where the overlapped curves showed that there was no significant saturation current degradation during the SC test process.

The experimental results reveal that DUT #1 could not achieve the 10-μs SCWT at the above test condition. As illustrated in Section I, the steeply elevated die temperature caused by the high saturation current at an 18-V gate voltage resulted in the low SCWT. Though by applying a lower gate voltage the SWCT could potentially be increased, the cost of increased conduction losses at normal operational conditions needs to be considered. For DUT #1, its saturation currents were measured at 18-V, 14-V, and 10-V gate voltages, as plotted in Fig. 5(a). The device's I-V characteristics at these three gate voltages are shown in Fig. 5(b). Table I summaries the peak SC currents, the SC energies, and the normal-operating turn-on resistances. According to Table I, for the baseline scenario with an 18-V gate voltage, the SC energy within 1 μs reduces by 40.6 % and 77.6 % using 14-V and 10-V gate voltages respectively, which suggests extended SCWTs. As the trade-off, the turn-on resistance increases by 18.0 % and 164.2 % with 14-V and 10-V gate voltages respectively. Therefore, keeping a constant lower gate voltage just for the purpose of extending the device SCWT may not be acceptable for this 3.3-kV SiC device. The three-step ultra-fast SC protection method is introduced in Section III which only lowers the gate voltage during SC fault conditions.

III. The Classic Three-Step Ultra-fast SC Protection Method and Its Extensions

The three-step ultra-fast SC protection design principle for the 3.3-kV SiC device case is referenced in [15]. Minor

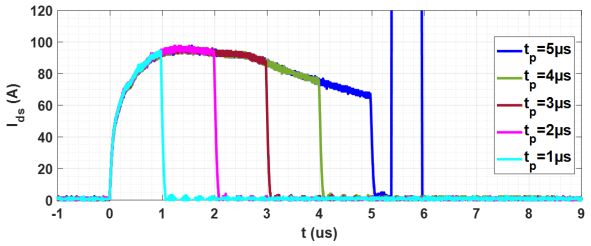
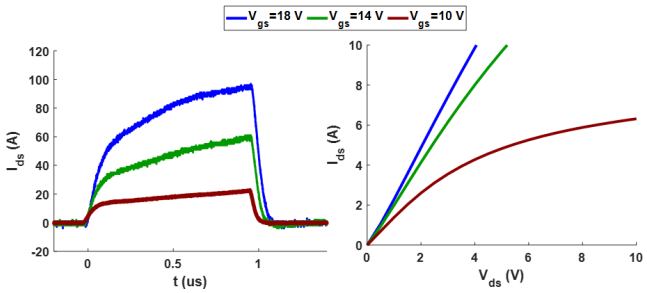


Fig. 4 DUT #1: the SC currents from the first to the fifth turn-on pulse.



(a) (b)

Fig. 5 At three different gate voltages: (a) DUT #1's saturation currents; (b) DUT #1's first quadrant I-V curves.

TABLE I
DEVICE'S CHARACTERISTICS AT DIFFERENT GATE VOLTAGES

Gate Voltage	Peak SC Current	Turn-on Energy during 1 μs	On Resistance at 5-A Current
10 V	22 A	37 mJ	1086 mΩ
14 V	61 A	98 mJ	485 mΩ
18 V	96 A	165 mJ	411 mΩ

modifications were made in insulation distances, detection signal filters, and drive circuit structures. The schematic for the lower device SC protection function is drawn in Fig. 6, in which the three steps include ultra-fast SC detection, active gate clamping, and DESAT detection with soft turn-off are highlighted. The ultra-fast detection is the first step and the detection sensing point is at the upper device's drain terminal. For the turn-on with normal current and the turn-on causing half-bridge shoot-through, different voltage behaviors can be extracted at this sensing point due to the differences in the decoupling capacitance voltage decreasing magnitudes and the voltage drops on the busbar stray inductor (different *di/dt* magnitudes). The simulated waveforms of these two scenarios are shown in Fig. 7, in which the sensed voltage signal after the filter can be compared with a preset reference voltage to diagnose whether a SC fault has occurred. Once the fault is diagnosed, the SW2 in Fig. 6 will be turned on for tens of microseconds to insert a gate voltage divider resistor, which is the second step. The lowered gate voltage can limit the device SC energy to reduce the risks of device degradation or failure. The output signal of the ultra-fast SC detection circuit can also be sent to the upper device's gate driver through a digital isolator to lower the upper device's gate voltage simultaneous. Following this the DESAT protection procedure (the third step) takes effect and softly turns off the device.

The detection method (the first step) shown above is one of the optional methods of tracking and indicating the transient energy changes at circuit elements that can display differences in a normal switching event and in a switching event with a SC

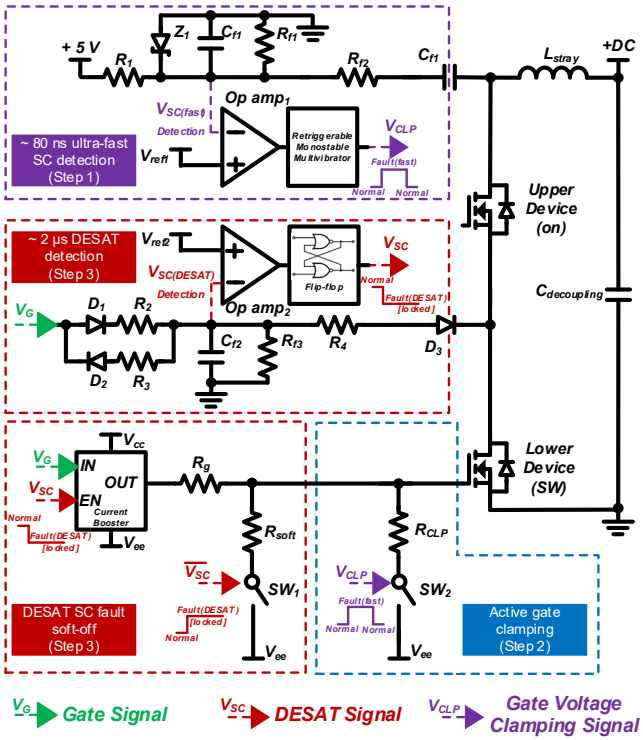


Fig. 6 Three-step ultra-fast SC protection schematic for the lower device's gate drive.

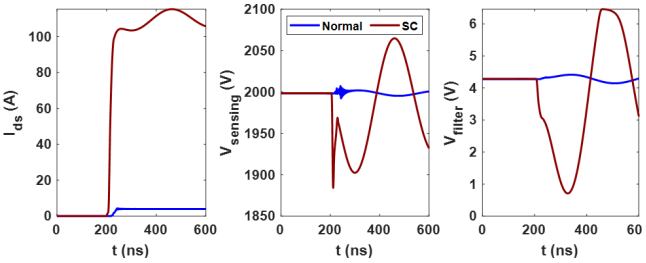


Fig. 7 Simulated waveforms under normal switching and half-bridge shoot-through: (a) device's drain-source current, (b) voltage oscillation at the sensing point, (c) the sensed voltage signal after the filter processing.

fault. Two more approaches [21], [22] can also be utilized as the first detection step, as shown in Fig. 8 in the case of a half-bridge shoot-through fault. In Fig. 8, when the lower device is turning on and cause a SC fault, due to the reduced voltage change between the lower device drain and source terminals, the Miller capacitance (C_{dg}) discharging current is largely eliminated, which causes reduced overall gate charge [21]. Meanwhile, a more significant voltage difference between the device's Kelvin source and source can be detected [22], which is based on the similar mechanism of [15], [16] but by utilizing the bond wire inductance rather than the busbar stray inductance. Theoretically, tens or hundreds of nanoseconds detection time could be achieved by all the above methods. By integrating one of these detection methods with the gate voltage clamping circuit and the DESAT protection circuit, a fast and robust SC protection function can be built.

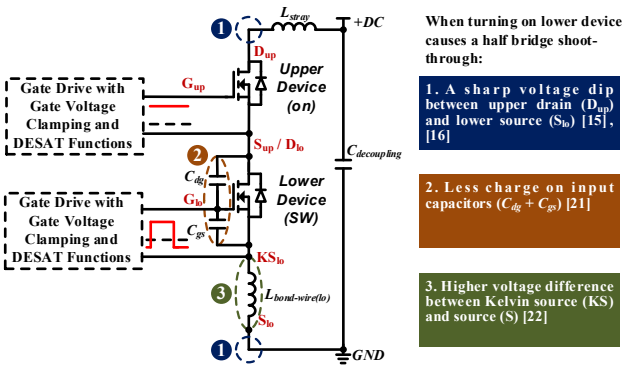


Fig. 8 SC detection methodologies based on transient energy changes.

IV. Experimental Validation of the Three-Step Ultra-Fast SC Protection

A half-bridge test setup was built with the upper device shorted as shown in Fig. 9. The circuit parameters in Fig. 2 and Fig. 9 are largely the same, except the shunt resistor was removed and a new gate drive integrating the three-step ultra-fast SC protection was used. The current was measured by the 30-MHz Rogowski coil in the protection validation test. The setup picture is shown in Fig. 10.

The 3.3-kV DUT #2 (the lower device) was tested under a 2-kV bus voltage with an 18-V preset turn-on gate voltage. The SC test result with protection is shown in Fig. 11. After 80 ns when the device was turned on, the fault flag of the ultra-fast SC detection was set. Then within several nanoseconds, the gate voltage dropped to 14 V and the slew rate of the drain-source current was reduced. Eventually, the desaturation protection circuit confirmed the fault and started a soft turn-off at 2.2 µs. Fig. 12 shows the saturation current comparisons with and without the gate clamping function using a 1-µs SC pulse. It shows a 32% reduction of the SC energy with the gate clamping function.

Additionally, a noise immunity for this ultra-fast detection method was verified by using a multi-pulse clamped inductive switching test with the same setup. Fig. 13 shows the noise immunity test waveforms. At a 2-kV dc bus voltage, with up to a 7-A load current, the ultra-fast SC detection was not falsely triggered. Therefore, under normal operation, the efficiency of the electrical system will not be influenced by the three-step ultra-fast SC protection function.

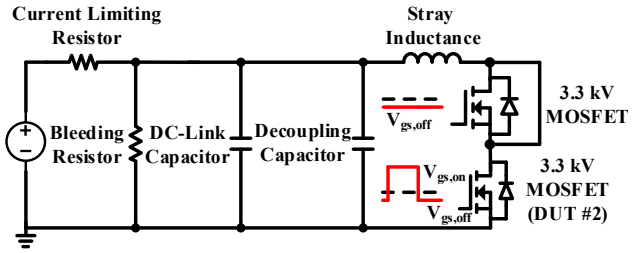


Fig. 9 SC protection test circuit for the 3.3-kV SiC MOSFET.

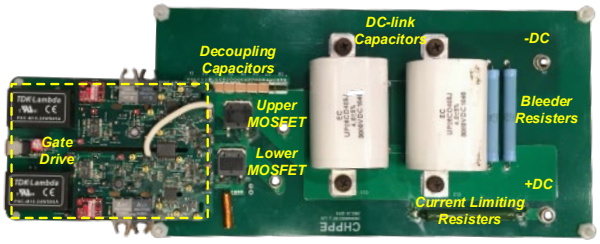


Fig. 10 Setup picture of the SC protection validation experiment.

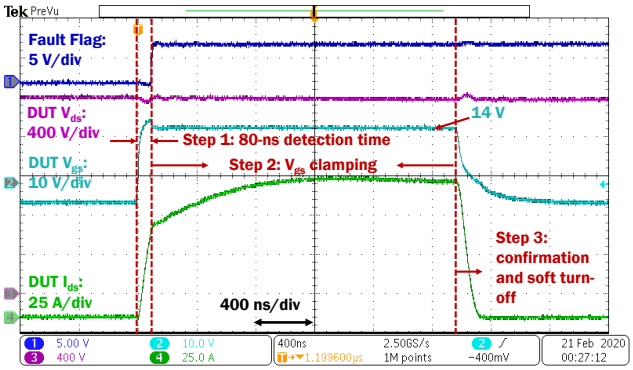


Fig. 11 DUT #2: SC test with the three-step ultra-fast SC protection.

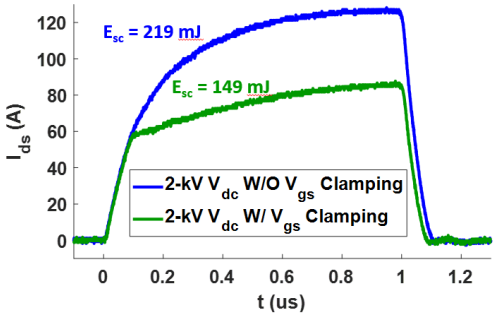


Fig. 12 DUT #2: saturation currents in 1-µs SC pulse with/without gate clamping function.

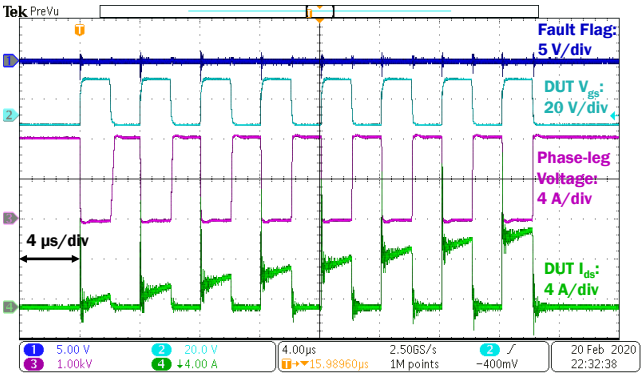


Fig. 13 DUT #2: multi-pulse clamped inductive switching test with the three-step ultra-fast SC protection.

V. Conclusion

This paper presents the SC capability evaluation of the 3.3-kV 5-A GeneSiC SiC MOSFET and the method to improve its SCWT. The SCWT of DUT #1 could not reach 10-µs at a 2.2-

kV bus voltage with an 18-V gate voltage. Though its SCWT could potentially be extended with 14-V or 10-V gate voltages, this can result in a significant increase of the DUT's on resistance in the normal operation area. A three-step ultra-fast SC protection method, which only reduces the gate voltage during SC faults was introduced. This method was validated by experiment. In the experiment, the device's gate voltage could be lowered within 80 ns and the SC energy could be reduced by around 32%. Furthermore, a noise immunity test showed this protection would not be falsely triggered at the device's rated current.

ACKNOWLEDGMENT

The authors would like to thank GeneSiC for providing 3.3-kV SiC engineering samples with various designs.

REFERENCES

[1] S. Madhusoodhanan, A. Tripathi, D. Patel, K. Mainali, A. Kadavelugu, S. Hazra, S. Bhattacharya and K. Hatua, "Solid-State Transformer and MV Grid Tie Applications Enabled by 15 kV SiC IGBTs and 10 kV SiC MOSFETs Based Multilevel Converters," in IEEE Transactions on Industry Applications, vol. 51, no. 4, pp. 3343-3360, July-Aug. 2015, doi: 10.1109/TIA.2015.2412096.

[2] A. Q. Huang, Q. Zhu, L. Wang and L. Zhang, "15 kV SiC MOSFET: An enabling technology for medium voltage solid state transformers," in CPSS Transactions on Power Electronics and Applications, vol. 2, no. 2, pp. 118-130, 2017, doi: 10.24295/CPSSTPEA.2017.00012.

[3] L. Zhang, R. Woodley, X. Song, S. Sen, X. Zhao and A. Q. Huang, "High current medium voltage solid state circuit breaker using paralleled 15kV SiC ETO," 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, USA, 2018, pp. 1706-1709, doi: 10.1109/APEC.2018.8341247.

[4] A. Verdicchio, P. Ladoux, H. Caron and C. Courtois, "New Medium-Voltage DC Railway Electrification System," in IEEE Transactions on Transportation Electrification, vol. 4, no. 2, pp. 591-604, June 2018, doi: 10.1109/TTE.2018.2826780.

[5] S. Madhusoodhanan, K. Hatua, S. Bhattacharya, S. Leslie, S. Ryu, M. Das, A. Agarwal and D. Grider, "Comparison study of 12kV n-type SiC IGBT with 10kV SiC MOSFET and 6.5kV Si IGBT based on 3L-NPC VSC applications," 2012 IEEE Energy Conversion Congress and Exposition (ECCE), Raleigh, NC, 2012, pp. 310-317, doi: 10.1109/ECCE.2012.6342807.

[6] X. Huang, L. Fursin, A. Bhalla, W. Simon and J. C. Dries, "Design and fabrication of 3.3kV SiC MOSFETs for industrial applications," 2017 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD), Sapporo, 2017, pp. 255-258, doi: 10.23919/ISPSD.2017.7988908.

[7] V. Mulpuri, S. Jadav, S. Sundaresan and R. Singh, "Characterization and Robustness Evaluation of 3.3 kV/40 mΩ SiC DMOSFETs," 2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Raleigh, NC, USA, 2019, pp. 130-136, doi: 10.1109/WiPDA46397.2019.8998847.

[8] Fairchild Semiconductor. IGBT Behavior under Short Circuit and Fault Protection. [Online]. Available: https://www.yumpu.com/en/document /read/11384505/igbt-behavior- under-short-circuit-and-fault-protection.

[9] E. Eni, S. Bęczkowski, S. Munk-Nielsen, T. Kerekes, R. Teodorescu, R. Juluri, B. Julsgaard, E. VanBrunt, B. Hull, S. Sabri and D. Grider, "Short-Circuit Degradation of 10-kV 10-A SiC MOSFET," in IEEE Transactions on Power Electronics, vol. 32, no. 12, pp. 9342-9354, Dec. 2017.

[10] J. Sun, J. Wei, Z. Zheng, Y. Wang and K. J. Chen, "Short Circuit Capability and Short Circuit Induced Vth Instability of a 1.2-kV SiC Power MOSFET," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 7, no. 3, pp. 1539-1546, Sept. 2019.

[11] X. Zhou, H. Su, Y. Wang, R. Yue, G. Dai and J. Li, "Investigations on the Degradation of 1.2-kV 4H-SiC MOSFETs Under Repetitive Short-Circuit Tests," in IEEE Transactions on Electron Devices, vol. 63, no. 11, pp. 4346-4351, Nov. 2016, doi: 10.1109/TED.2016.2606882.

[12] T. Nguyen, A. Ahmed, T. V. Thang and J. Park, "Gate Oxide Reliability Issues of SiC MOSFETs Under Short-Circuit Operation," in IEEE Transactions on Power Electronics, vol. 30, no. 5, pp. 2445-2455, May 2015.

[13] H. Hatta, T. Tominaga, S. Hino, N. Miura, S. Tomohisa, and Y. Yamakawa, "Suppression of Shor-Circuit Current with Embedded Source Resistance in SiC-MOSFET", Int. Conf. on Silicon Carbide and Related Materials, 2017.

[14] A. Kanale and B. J. Baliga, "A New User-Configurable Method to Improve Short-Circuit Ruggedness of 1.2-kV SiC Power MOSFETs," in IEEE Transactions on Power Electronics, vol. 36, no. 2, pp. 2059-2067, Feb. 2021, doi: 10.1109/TPEL.2020.3010154.

[15] X. Lyu, H. Li, Y. Abdullah, K. Wang, B. Hu, Z. Yang, J. Liu, J. Wang, L. Liu, and S. Bala, "A Reliable Ultra-fast Short-Circuit Protection Method for E-Mode GaN HEMT," in IEEE Transactions on Power Electronics, vol. 35, no. 9, pp. 8926-8933, Sept. 2020, doi: 10.1109/TPEL.2020.2968865.

[16] K. Wang, Y. Abdullah, X. Li, D. Xing, J. Wang, L. Liu, and S. Bala, "A Reliable Short-Circuit Protection Method with Ultra-Fast Detection for GaN based Gate Injection Transistors," 2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Raleigh, NC, USA, 2019, pp. 43-46, doi: 10.1109/WiPDA46397.2019.8998869.

[17] A. Pérez-Tomáset, P. Brosselard, P. Godignon and J. Millán, "Field-effect mobility temperature modeling of 4H-SiC metal-oxide-semiconductor transistors," Journal of Applied Physics, vol. 100, no. 11, p. 114508, 2006.

[18] P. Gaubert, A. Teramoto, S. Sugawa and T. Ohmi, "The role of the temperature on the scattering mechanisms limiting the electron mobility in metal-oxide-semiconductor field-effect-transistors fabricated on (110) silicon-oriented wafers," 2012 Proceedings of the European Solid-State Device Research Conference (ESSDERC), Bordeaux, 2012, pp. 213-216, doi: 10.1109/ESSDERC.2012.6343371.

[19] K. Han, A. Kanale, B. J. Baliga, B. Ballard, A. Morgan and D. C. Hopkins, "New Short Circuit Failure Mechanism for 1.2kV 4H-SiC MOSFETs and JBSFETs," 2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Atlanta, GA, 2018, pp. 108-113.

[20] G. Romano, A. Fayyaz, M. Riccio, L. Maresca, G. Breglio, A. Castellazzi and A. Irace, "A Comprehensive Study of Short-Circuit Ruggedness of Silicon Carbide Power MOSFETs," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 3, pp. 978-987, Sept. 2016.

[21] T. Horiguchi, S. Kinouchi, Y. Nakayama and H. Akagi, "A fast short-circuit protection method using gate charge characteristics of SiC MOSFETs," 2015 IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, QC, 2015, pp. 4759-4764, doi: 10.1109/ECCE.2015.7310332.

[22] Z. Wang, X. Shi, L. M. Tolbert, F. Wang and B. J. Blalock, "A di/dt Feedback-Based Active Gate Driver for Smart Switching and Fast Overcurrent Protection of IGBT Modules," in IEEE Transactions on Power Electronics, vol. 29, no. 7, pp. 3720-3732, July 2014, doi: 10.1109/TPEL.2013.2278794.