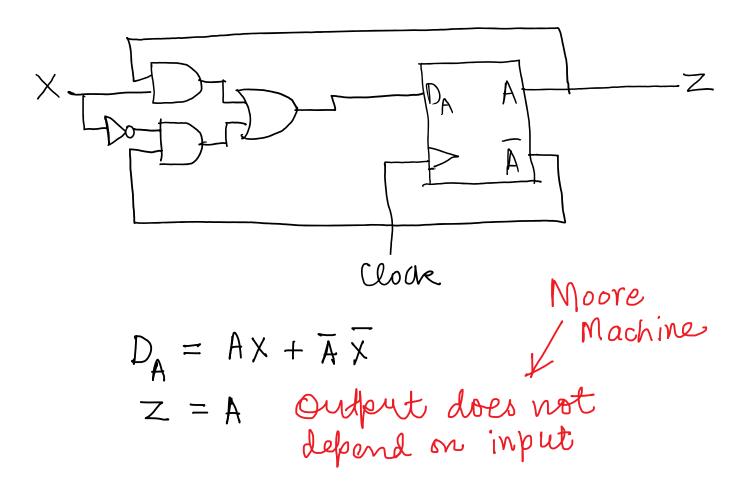
## MT2 Solutions ECE2060 Sp 2022

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**Problem 1 (30 points):** Consider the circuit in the figure below.

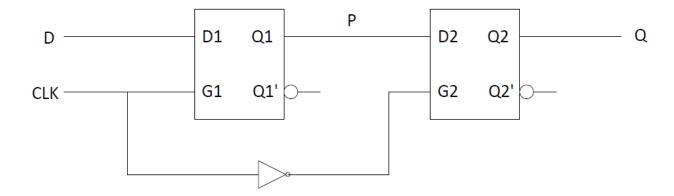
- i) Is this a Mele or Moore machine?
- ii) Draw the state graph corresponding to this circuit

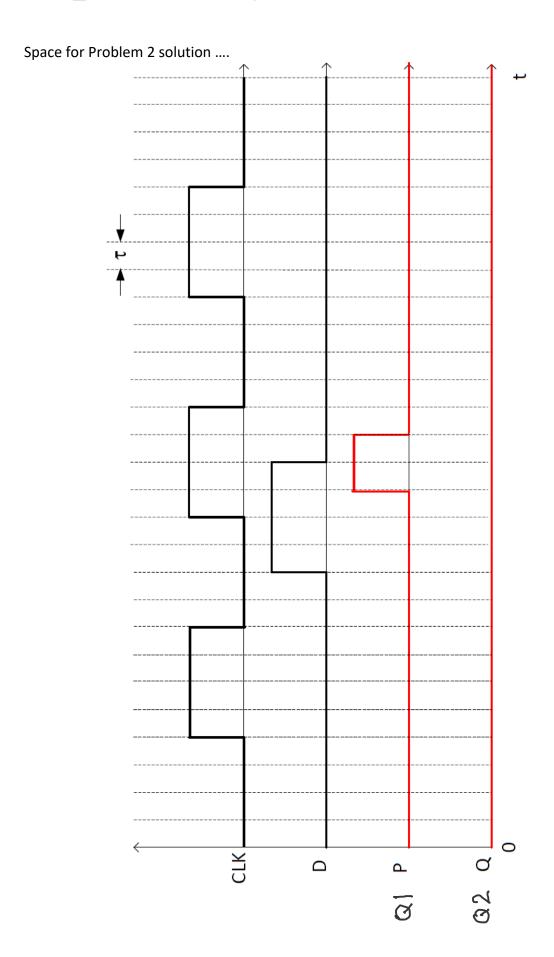


| Space for Problem 1 solution |          |   |     |     |     |                             |  |  |  |  |  |
|------------------------------|----------|---|-----|-----|-----|-----------------------------|--|--|--|--|--|
| <u></u>                      | <b>†</b> | X | DA  | ATT | 7.t | $A^{\dagger} = D_A$ $Z = A$ |  |  |  |  |  |
| /0                           | )        | D | 1   | [   | 0   | L-N                         |  |  |  |  |  |
|                              |          |   | 0   | O   | Ō   |                             |  |  |  |  |  |
|                              |          | 0 | 0   | 0   | \   |                             |  |  |  |  |  |
|                              |          |   | 1   |     | (   |                             |  |  |  |  |  |
|                              |          |   | 1 ' | ,   |     |                             |  |  |  |  |  |
|                              |          |   |     |     |     |                             |  |  |  |  |  |
|                              |          |   |     |     |     |                             |  |  |  |  |  |
|                              | (        |   | 00  |     |     | r                           |  |  |  |  |  |
|                              | \        |   |     | ~ O |     |                             |  |  |  |  |  |

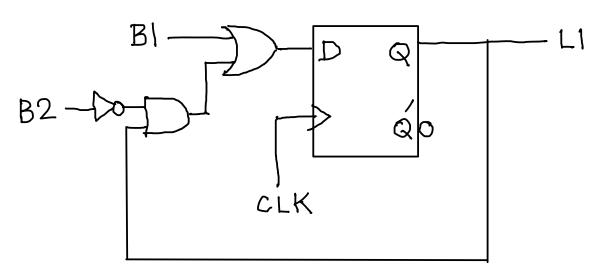
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**Problem 2 (35 points):** Consider the circuit in the figure below containing two **gated D latches**. Given the timing diagrams of CLK and D in the graph on the next page, complete the timing diagrams for Q1 and Q2. Consider that the latches have a delay of  $\mathcal{L}$  and the not-gate has zero delay. Assume that Q1 = 0 at t = 0. **Note:** The two components in this circuit are **Gated D-Latches**, not D Flip-Flops.





**Problem 3 (35 points):** Consider the circuit in the figure below containing a D Flip-Flop. Given the timing diagrams of CLK, B1 and B2 in the graph given on the next page, complete the timing diagrams for D and Q. Consider that the Flip-Flop has a delay of  $\Upsilon$  and the gates have zero delay. Assume Q = 0 at t = 0.



Easear to do the timing diagram by figuring out the state table first

|   |    |    | 7 [ | $= \mathbf{E}$       | 31+            | B2·Q = D |
|---|----|----|-----|----------------------|----------------|----------|
| Q | BI | B2 | D   | Q <sup>+</sup>       | LI             | L1=Q     |
| 0 | O  | Ь  | 6   | <b>\( \lambda \)</b> | 0              |          |
| O | O  | 1  | 6   | 0                    | 0              |          |
| 0 | 1  | O  |     | 1                    | O              | B1+B2    |
| Ø | 1  | l  |     | 1                    | 0              |          |
| 1 | 0  | •  | 1   | 1                    |                |          |
| l | ٥  | 1  | O   | 0                    | \ <sub>1</sub> |          |
| 1 | J  | 0  | l   | 1 1                  | t 1            |          |
| J | J  | ?  | 1   |                      | 1              |          |

