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Recently there has been much interest generated around tunnel junctions (TJs) for applications in III-Nitride optoelectronics. TJs could enable multiple active region emitters that provide a promising solution to realize high power density without efficiency droop[1]. There has not been a detailed physics-based understanding of tunneling physics in III-Nitride LEDs and key questions must be answered. Our work aims to answer key design questions related to voltage and resistance losses in GaN tunnel junctions, especially under design constraints set by MOCVD growth limitations. We use simulations to design and engineer transparent graded InGaN tunnel junctions, and demonstrate that these simulations can predict experimentally observed resistance and voltage penalty. We also use simulations to design graded InGaN TJs with state-of-art low voltage penalty of 0.19 V at 100 A/cm^2, the lowest measured value for an all-MOCVD approach.

Modeling: We use a standard device simulator (Silvaco Atlas) with a nonlocal band to band tunneling model to gain physical insight into the design tunnel junctions. By considering the origin of the voltage drop in III-Nitride TJs it is possible to identify design parameters which can be manipulated to achieve the required low V_{TJ} for a cascaded LED. Starting with the GaN homojunction TJ, which consists of a simple heavily doped p++/n++ junction, we identify depletion width and the Fermi level position in the p-type GaN as key design parameter.

The use of graded InGaN interlayers near the tunnel junction interface enables us to achieve higher Mg activation, which enable higher tunneling rates between the heavily doped p++GaN and n++GaN. Simulations help to understand the effect of the non-degeneracy in p++GaN which leads a large energy difference between the Fermi level and valence band. This leads to a voltage drop required to align the valence band states on the p-side of the tunnel junction with the conduction band states on the n-side. In contrast, electrostatic ionization of graded p-InGaN leads to near-degenerate p-InGaN, which enables a reduced voltage for onset of tunneling. Simulations directly provide quantitative comparison of tunneling rates, both as a function of design and as a function of applied voltage. As the operating voltage of the TJ increases, the tunneling distance decreases and the band to band tunneling rates increase. We show how the thickness of the graded InGaN interlayer impacts the V_{TJ}.

Experiment: We compare the models developed here with experimental results. We have used a simulation-driven approach to design experiments for monolithic growth by MOCVD. Tunnel junctions were grown on top of a standard pn-diode containing a thick n+GaN template, a 200nm n-GaN layer with [Si]=$2\text{x}10^{16}$ cm^{-3}, and a 90nm p+GaN layer with [Mg]=$3\text{x}10^{19}$ cm^{-3}. The GaN homojunction TJ contains a 12nm p++GaN layer with [Mg]=$2\text{x}10^{20}$cm^{-3} followed by a 10nm n++GaN layer with [Si]=$3\text{x}10^{20}$cm^{-3}, and finally a 500nm n+GaN contact layer. The graded InGaN interlayer TJs contain a 12nm (or 6nm) p++GaN layer with [Mg]=$2\text{x}10^{20}$ cm^{-3} followed by a p++InGaN layer graded from 0% to 10% In mole fraction and [Mg]=$4\text{x}10^{20}$cm^{-3}. Next a n++InGaN layer graded from 10% to 0% In mole fraction and [Si]=$4\text{x}10^{20}$cm^{-3} followed by a n++GaN layer with [Si]=$3\text{x}10^{20}$ cm^{-3} and finally a 500nm n+GaN contact layer. The devices were compared to a control pn-diode to extract V_{TJ}. These TJs were measured to have V_{TJ}=0.19V and V_{TJ}=0.47V at current density of 100 A/cm^2 for the graded InGaN interlayer TJ and the GaN homojunction TJ, respectively. In comparison, the expected values from modeling are V_{TJ}=0.26V for InGaN interlayer TJ and V_{TJ}=0.56V for GaN homojunction TJ. This shows that standard device models give key insight into the ultimate limits of tunnel junctions, and can provide a powerful way to design and predict the performance of tunnel junctions.

[1] Akyol, F., Krishnamoorthy, S., Rajan, S. (2013). *Applied Physics Letters*, *103*(8), 081107.

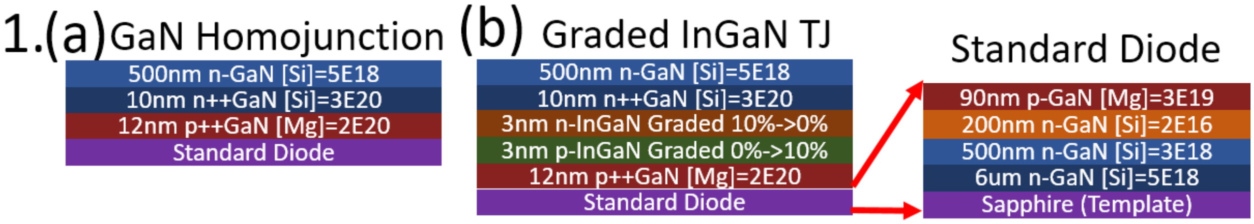

Fig. 1. a) The schematic of the GaN homojunction grown on a standard pn-diode. The GaN homojunction consists of a heavily doped p++GaN/n++GaN junction. **b)** The schematic of the graded InGaN interlayer tunnel junction which includes a graded InGaN interlayer between the heavily doped p++GaN and n++GaN. In this design a p++ InGaN layer is graded from 0% to 10% In mole fraction on the p-side of the TJ, and a n++ InGaN layer is then graded from 10% to 0% In mole fraction on the n-side of the TJ.

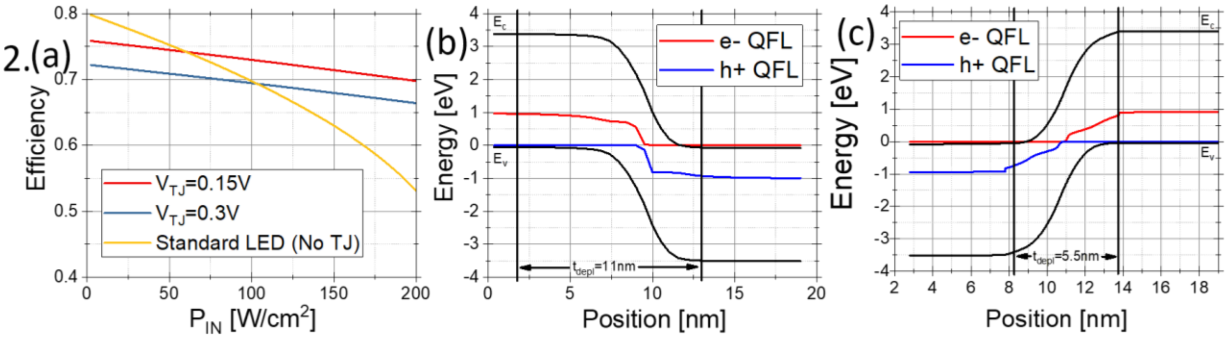

Fig. 2. a) A plot of efficiency versus input power for a 3x multi-junction LED with varying voltage drop across the tunnel junction (V_{TJ}) as compared to a standard single LED with no tunnel junction. The figure shows the point where the 3x cascaded LED becomes more efficient than the standard LED. **b)** The band diagram of the homojunction tunnel junction design, and **c)** the graded InGaN interlayer tunnel junction design. The depletion width for the graded InGaN interlayer TJ (5.5nm) is half that of the GaN homojunction (11nm).

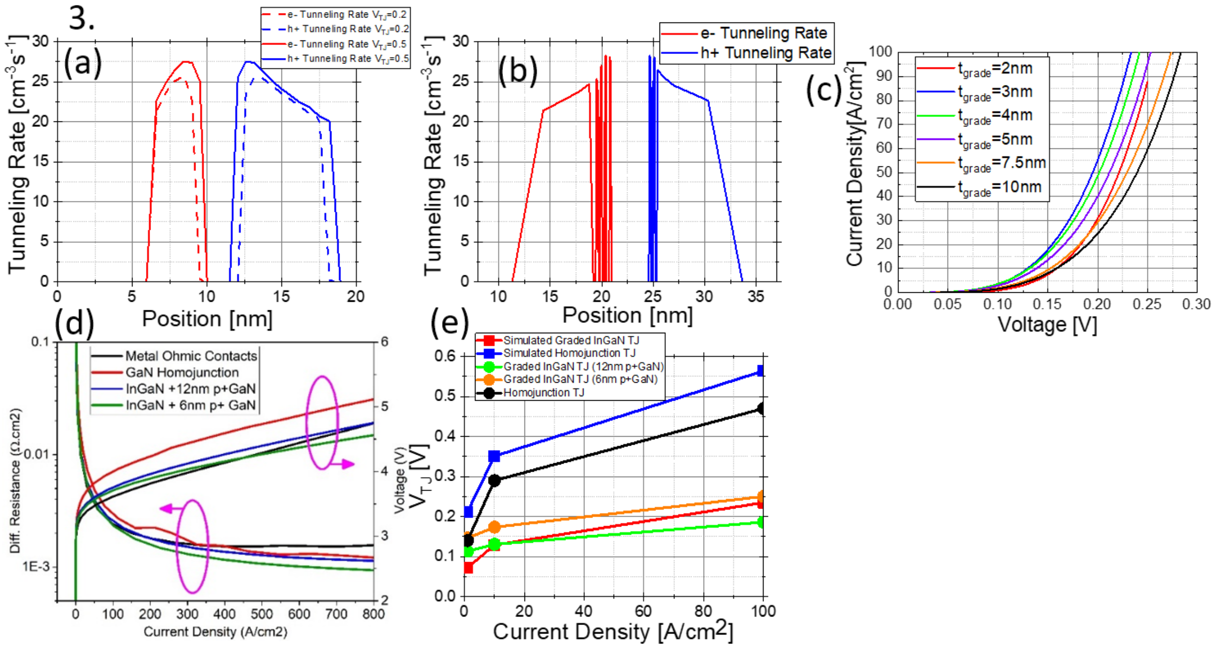

Fig. 3. a) A plot of the nonlocal band to band tunneling (BBT) rates of electrons (shown in red) and holes (shown in blue) for the GaN homojunction TJ. The dashed lines indicate an applied bias across the tunnel junction of V_{TJ}=0.2V. The solid lines indicate V_{TJ}=0.5V for the GaN homojunction TJ. **b)** The BBT rates in the graded InGaN interlayer TJ for V_{TJ}=0.2V. It can be seen that the tunneling rates for the graded InGaN interlayer TJ at V_{TJ}=0.2V are comparable to the GaN homojunction at V_{TJ}=0.5V. c) Simulated J-V characteristics for the graded InGaN interlayer TJ with various grading thicknesses. **d)** The measured differential resistance vs current density (left axis) and voltage vs current density (right axis) for the various tunnel junction designs grown monolithically by MOCVD. **e)** The voltage drop across the tunnel junction (V_{TJ}) at J= 1, 10, 100 A/cm^2 for the simulated GaN homojunction (blue line), the experimental GaN homojunction (black line), the simulated graded InGaN interlayer TJ (red line), the experimental graded InGaN interlayer TJ with a 6nm thick p++GaN layer (orange line), and the experimental graded InGaN interlayer TJ with a 12nm thick p++GaN layer (green line).