JVSTB Journal of Vacuum Science & Technology B

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Citation: Journal of Vacuum Science & Technology B **32**, 02C111 (2014); doi: 10.1116/1.4865477
View online: http://dx.doi.org/10.1116/1.4865477
View Table of Contents: http://scitation.aip.org/content/avs/journal/jvstb/32/2?ver=pdfcov
Published by the AVS: Science & Technology of Materials, Interfaces, and Processing

Selectively grown GaAs nanodisks on Si(100) by molecular beam epitaxy

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(Received 12 November 2013; accepted 30 January 2014; published 18 February 2014)

The authors report the molecular beam epitaxial growth and the structural and optical characterizations of self-assembled/catalyst-free GaAs nanodisks on SiO_2 masked Si(100) patterned substrates. Pure zincblende GaAs nanodisks with precise positioning and low defect density are demonstrated by selective area epitaxy. The influence of the growth temperature and deposition duration is investigated. Excellent morphological and structural properties are characterized by scanning electron microscopy and cross-sectional transmission electron microscopy. Defects in the epilayers are reduced by strain relaxation through facets formation and by a lateral overgrowth scheme atop the SiO_2 mask which is corroborated by microRaman spectroscopy. In particular, the authors show how the material quality contributes to excellent optical properties observed by microphotoluminescence spectroscopy from 77 K to room temperature. © *2014 American Vacuum Society*. [http://dx.doi.org/10.1116/1.4865477]

I. INTRODUCTION

III-V epitaxial nanostructures including nanowires, quantum dots, etc., are key enablers for nanotechnologies, and some achievements have already been demonstrated in nanoelectronics,[1] nanophotonics,[2] biosensors,[3,4] and so on. The inherent merits in high electron mobilities, direct bandgaps, and vast possibilities of bandgap engineering are the main reasons to make these nanostructures sought-after. High-quality of such nanostructures can be easily obtained through homoepitaxy by molecular beam epitaxy (MBE), metalorganic chemical vapor deposition, or chemical beam epitaxy. However, it is desirable to have such high quality III-V nanostructures integrated to the cost-effective and complementary metal oxide semiconductor (CMOS) compatible Si platform. In fact, successful heteroepitaxial growth will not only provide high carrier mobility and direct bandgap III-V materials, but also maintain the advantages of lightweight and low-cost Si substrates with high mechanical strength and excellent thermal management. *To date*, researchers have extensively focused on the growth of high quality III-V compounds on Si and tried to accomplish the so-called bottom–up integration. Due to the mismatches in lattice constants, thermal expansion coefficients, and polar/nonpolar nature, the misfit dislocations, threading dislocations, and antiphase domain boundaries (APB) are generated, which results in tremendous degradation of the device electrical and optical properties. Although various growth schemes such as complex thermal cycle annealing process,[5–7] strained layer superlattice buffer layers,[8] micron-thick graded buffer layers,[9] microchannel epitaxy,[10] flow-rate modulation epitaxy, and migration-enhanced epitaxy[11,12] have been developed, they still have not efficiently elimintated the aforementioned defects. More remarkably, these defects play key roles to hinder the possibility to realize the high-efficieny minority carrier devices like light emitting diodes, laser diodes, and avalanche photodiodes on Si.

In this context, we investigate our growth of self-assembled/catalyst-free GaAs nanodisks on top of SiO_2 masked Si(100) patterned substrates by molecular beam epitaxy. With the assist of the selective area epitaxy (SAE) on patterned substrates, the stress is laterally relaxed through the top facet and side wall formation, leading to nearly defect-free GaAs nanodisks. Most importantly, this growth scheme can effectively mitigate the major mismatch problems based on the finite size growth condition. The finite size growth leads to the reduction in the thermal stress at GaAs/Si interface, therefore minimizing the formation of threading dislocations and stacking faults penetrating into the epilayers. Furthermore, instead of using misoriented Si substrates, this SAE approach using nominal Si(100) substrates could also effectively reduce the probability of forming high-density APBs. On top of that, (100) oriented substrate is compatible with the mainstream CMOS technology, which enables us to fulfill the genuine III-V to Si platform integration. In addition to all these obvious advantages, the SAE growth technique eliminates the need for patterning postgrowth mesas, while the SiO_2 sidewalls can automatically serve as a lateral electrical isolation. As for the catalyst-free growth mechanism for our GaAs nanodisks, the lack of seed particles

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avoids the diffusion of the seed on/into Si and forbids the creation of detrimental deep level traps or scattering centers in GaAs and Si. Thus, these merits enable a viable pathway to integrate three dimensional based GaAs nanostructure devices to Si-based processes and electronics. We hereby report the selectively grown GaAs nanodisks on Si(100) substrates with a *substantially reduced* number of *defects*. The key influences of the growth temperature and deposition duration are investigated. The precise positioning process were defined using hole arrays with SiO_2 on Si(100) substrates. Rectangular GaAs nanodisks with superior material quality were formed due to the strain relaxation through facets and lateral overgrowth. Cross-sectional transmission electron microscopy investigation reveals the single crystalline zinc-blende structure and the reduced number of stacking faults and dislocations. Micro-Raman spectroscopy indicates the GaAs nanodisks crystallinity changes from polycrystal-dominant to single crystal-dominant structure from the growth temperature at 550 °C–630 °C. Besides, the strong direct band-to-band transition from microphotoluminescence (μ-PL) spectroscopy demonstrates the catalyst-free growth mechanism successfully circumvent the incorporation of such midgap trap centers.

II. EXPERIMENTAL DETAILS

First, a 60nmthick SiO_2 was thermally grown on Si(100) substrates. Arrays of circular holes with a diameter of 1 μm were defined by stepper lithography followed by the subsequent inductive coupled plasma reactive ion etching (RIE) of the top SiO_2 layer. Prior to the growth, the patterned substrates are chemically cleaned. They were degreased sequentially in acetone, isopropyl alcohol with ultrasonic agitation, and treated in 30% KOH for 20 s at room temperature to remove the RIE damaged Si surface and expose a fresh Si surface in the patterned holes. Then, the patterned substrates were cleaned by piranha solution (H_2SO_4:$H_2O_2 = 1$:3) for 3 min at room temperature. Immediately prior to loading the patterned substrates to the MBE loadlock, a 30-s dip in 5% diluted hydrofluoric acid solution was done to remove the native oxide on the exposed silicon surface and achieve hydrogen passivation, then rinsed in deionized water for 1 min and blown dry with nitrogen. The cleaned samples were further degassed at 400 °C for 10 min in the buffer tube of our Perkin-Elmer 430 MBE system prior to loading into the growth chamber. Afterwards, the thermal treatment was applied at 900 °C for 10 min in the MBE growth chamber to desorb residual native oxides, which might have formed during the loading, and to make the surface hydrogen-free. In order to enable growth runs start with the most stable growth condition, all of the growth runs were initiated exposing the patterned substrates under the As_2 overpressure for 5 min to turn the exposed Si surface inside the patterned circular holes into the As-terminated one. Subsequently, the growth of high quality GaAs layers on Si was performed under an As_2 beam equivalent pressure around 2×10^{-6} Torr. Thermocouple and pyrometer were simultaneously used to measure the growth temperature. The two-dimensional (2D) equivalent growth rates and V/III ratios were calculated and calibrated by reflection high energy electron diffraction similar to GaAs homoepitaxy.

We initiated the growth by depositing a low temperature grown 25 nm-thick GaAs layer at 400 °C to reduce the unintentional doping effect from the Si atoms in the substrates. Followed by this stage, the growth of self-assembled/catalyst-free GaAs nanodisks then thereby started. The growth temperature dependent experiments were carried out from 550 °C to 630 °C with the V/III ratio at 10 to investigate the optimal growth temperature for SAE to take place. The As and Ga shutters were then simultaneously opened to initiate growth. The growth condition is similar to that of GaAs homoepitaxy with a Ga flux planar growth rate of 1 Å/s. After deposition of nominal 1 μm-thick GaAs, the growth was terminated. It was found that a growth temperature of 630 °C yields the best selectivity and crystal quality. Therefore, the time evolution study was also performed at this growth temperature to investigate the morphology change in each stage from the growth duration of 30–120 min.

The morphology of as-grown GaAs nanodisks was evaluated by scanning electron microscopy (SEM, JEOL, JSM-6700F, operated at 10 kV). The structural and crystalline quality was further investigated by cross-sectional transmission electron microscopy (XTEM, JEOL, JEM-3000F, operated at 300 kV). In addition, the micro-Raman spectroscopy (Renishaw Raman microscope) was performed at room temperature by using a 532 nm excitation laser. Finally, the temperature dependent μ-PL spectroscopy was performed under the excitation of 488 nm line Ar-ion laser at the power density of 6 W/cm^2, and the PL signal were detected by liquid-nitrogen cooled InGaAs detector.

III. RESULTS AND DISCUSSION

A. Catalyst-free and selective area epitaxy growth mechanisms

In the GaAs/Si low-dimensional nanostructures heteroepitaxy, one should consider not only the conventional problems relating to the major mismatches mentioned earlier, but also the following two questions: unintentional doping from the Si substrate, and misfit dislocation at the heterointerface. In the traditional vapor–liquid–solid growth of nanostructures, the seed catalysts usually corrosively etch the Si surface and release Si atoms which can diffuse into the epilayers.[13] For the catalyst-free growth, Si can also diffuse into GaAs epilayers because of the high growth temperatures required for the growth. This unintentional doping from the Si substrate is viewed to form a gradual carrier distribution layer inside the GaAs epilayers. In such a case, highly doped *n*-type layers may form close to the heterointerface resulting from the unintentional doping degrading the performance in GaAs nanostructures. Therefore, it is significant to suppress the unintentional doping. Although there have not been found the most effective and guaranteed way to suppress this kind of doping. It is believed a low-temperature grown buffer layer could probably suppress the unintentional

doping. Therefore, the growth was initiated by depositing a 25 nm-thick GaAs layer at 400 °C prior to the self-assembled/catalyst-free GaAs nanodisks. On the other hand, the intrinsically lattice-mismatched system usually introduces misfit dislocations at the heterointerface. However, these misfit dislocations could be effectively reduced by shrinking the contact area of the GaAs epilayer to the Si surface. Obviously, this is the advantage of the finite size SAE we applied in this study. In SAE, the growth is constrained in certain areas of a substrate, i.e., the one-dimensional (1D) growth is enhanced by suppressing the 2D growth.

The growth mechanism is schematically drawn in Fig. 1. Basically, a Si substrate is covered by an amorphous SiO_2 thin film patterned with micro- or nanoscale windows. Then, the growth conditions are chosen such that the sticking coefficients of the As and Ga adatoms are zero on SiO_2 and nonzero in the hole arrays, i.e., the exposed Si surface.[14] The purpose of SAE is to constrain the incorporation of group-III adatoms to certain areas on a patterned substrate. In fact, there are mainly two contributions that influence this growth mechanism: (1) diffusion of adatoms from SiO_2 to the exposed Si surface, and (2) preferential desorption of adatoms on SiO_2 relative to the Si surface. These two contributions to SAE are discussed theoretically as follows:

1. Diffusion of adatoms from the oxide

Based on the different lifetimes of adatoms before incorporation in a film or desorption from the substrate, there exists a concentration gradient over the edge between exposed Si surface and SiO_2. This gradient results in a net diffusion of Ga from SiO_2 to the exposed Si surface. Invoking the second Fick's law, we can describe the surface diffusion in the following differential equation:[15]

$$\frac{d\sigma}{dt} = D\left(\frac{d^2\sigma}{dx^2} + \frac{d^2\sigma}{dy^2}\right) - \frac{\sigma}{\tau} + R, \tag{1}$$

with $\sigma(x,y)$ being the surface density of adsorbed Ga atoms at a point on the 2D surface, $D(x,y)$ the coefficient of surface diffusion, $\tau(x,y)$ the lifetime of Ga adatoms on the surface, and R the incoming beam flux. This equation is now solved using necessary boundary conditions for periodic hole arrays in a SiO_2 layer with a hole pitch d. Then, the resulting σ is averaged over a hole, which would be proportional to the average nanostructure height. Unfortunately solving this approach would most likely require numerical methods. The surface lifetime τ of Ga adatoms is determined by the lifetime τ_i for incorporation into the surface and τ_d for desorption from the substrate. τ can be calculated from τ_i and τ_d according to Matthiessen's rule

$$\frac{1}{\tau(x,y)} = \frac{1}{\tau_i(x,y)} + \frac{1}{\tau_d(x,y)}. \tag{2}$$

Therefore, we now consider some approximations to get an analytical solution. Due to the radial symmetry of the holes, the concentration gradient at a position is assumed to be a point toward the center of the nearest neighboring Si hole. The diffusive transport on the oxide is characterized by a diffusion length L_D, which is the scale where only a $1/e$ fraction of the diffusive particles remain as the rest have desorbed from or incorporated to the substrate after this distance. Incorporation of Ga onto the oxide is neglected as this is not a significant effect in the selective growth regime. Meanwhile, the incorporation of atoms into the GaAs layer is considered to happen homogeneously over the exposed Si surface and at a high efficiency.

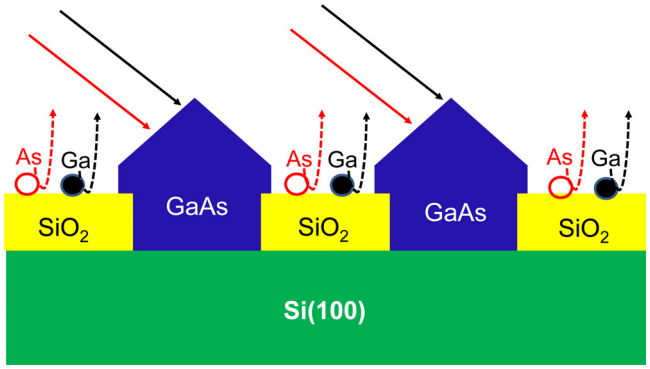

FIG. 1. (Color online) Schematic of growth mechanism for SAE displaying the diffusion and desorption of Ga/As adatoms atop the SiO_2 mask.

2. Desorption of adatoms on the oxide

The second contribution to selective growth results from a higher volatility of Ga and As adatoms on SiO_2 with respect to Si surfaces. The reason of this volatility is that the sticking coefficient of Ga and As adatoms on the SiO_2 surface is reduced with respect to the sticking probability on the GaAs surface because of less favorable binding sites. In particular, this also means that the growth of GaAs on the surface of the oxide also depends strongly on the existence of nucleation centers where diffusing Ga atoms become attached. In experimental situations, the sticking coefficient on SiO_2 is not completely zero eventually leading to the growth of polycrystalline GaAs on the oxide. Assuming quasiequilibrium conditions, the equation describing the maximum critical flux of impinging atoms leading to zero-deposition of GaAs on the SiO_2 surface is[16]

$$J_C \propto \frac{v_0^2}{4D_0} e^{-(2E_{Des}-E_{Diff})/k_BT}, \tag{3}$$

with v_0 being the desorption rate constant, D_0 the diffusion constant, E_{Diff} the activation energy for diffusion, E_{Des} the activation energy for desorption, and J_C is the critical flux for a given temperature T, below which zero-deposition occurs. As commonly $2E_{Des} - E_{diff} > 0$ in thin film growth, zero-deposition on the oxide is available by either increasing the growth temperature T at a given Ga-flux J_{Ga} or by decreasing the Ga-flux (deposition rate) J_{Ga} at a given temperature T.[16]

B. Experimental results

In order to investigate the mechanism of SAE, the growth-temperature dependent study was carried out to

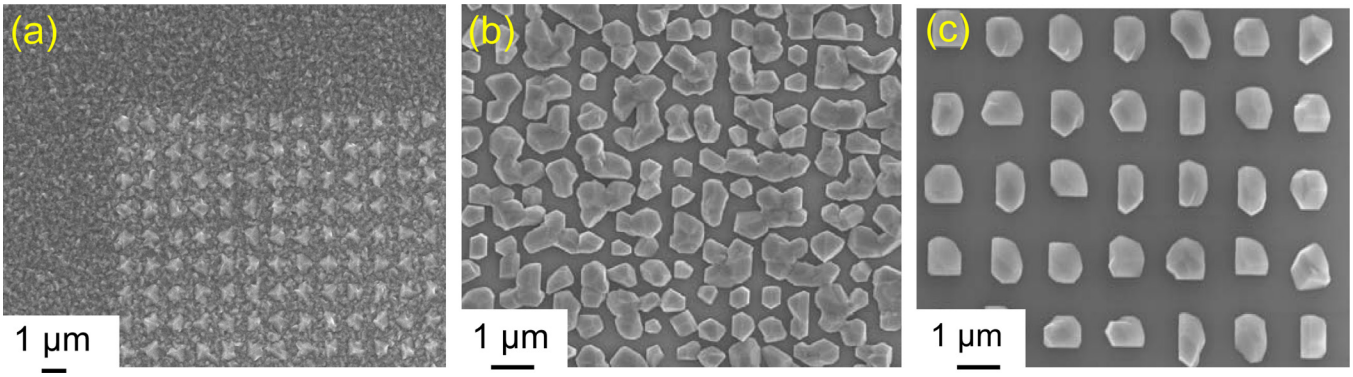

FIG. 2. (Color online) SEM images of growth temperature dependent study for SAE grown GaAs nanodisks on Si(100) patterned substrates at (a) 550 °C, (b) 600 °C, and (c) 630 °C.

understand the process of diffusion and desorption of Ga and As adatoms with respect to the exposed Si surface. Figure 2 shows three SEM micrographs of GaAs grown on patterned Si(100) substrates at growth temperatures ranging from 550 °C to 630 °C. The nominal deposition thickness is fixed at 1 μm for all of the growth runs. When the temperature is set at 550 °C as shown in Fig. 2(a), almost no selectivity is observed and the deposited GaAs exhibits amorphous or polycrystalline crystallites. As the temperature is increased to 600 °C as displayed in Fig. 2(b), rectangular crystals are formed at the patterned hole arrays sites, showing enhanced material quality with some top facets. Nevertheless, the selectivity is not as perfect as GaAs can still be seen on the SiO_2 surface and some agglomeration of GaAs crystallites between different pattern holes.

The complete selective growth is achieved at 630 °C as can be seen in Fig. 2(c). GaAs nanodisks preferentially fill the patterned holes to form the nanodisk arrays. Each individual nanodisk, as shown in Fig. 2(c), has lateral dimensions of ~1 μm as it fully covers the exposed Si surface. Faceting is very evident at this temperature, indicating single crystalline growth, although defects can still be observed on some of the crystals. It is noticeable that growth temperature significantly affects selectivity and material quality through adatom kinetics. A proper growth temperature of 630 °C is crucial to achieve the high material quality and the selective growth. However, when the substrate temperature is above 650 °C, the strong desorption of the selectively grown nanodisks predominates and no material is seen on either the exposed silicon surface or SiO_2. Otherwise, at low temperatures, selectivity becomes poor as polycrystalline GaAs crystallites were deposited both in the holes and on the mask surface as displayed in Fig. 2(a). The reason for the poor selectivity is because the diffusion length of Ga as well as the decomposition rate of GaAs on SiO_2 becomes much less than the higher temperature cases. Consequently, nucleation occurs on both of the patterned hole arrays and the mask. Furthermore, inside the patterned holes, the density of GaAs nucleation sites increases as a result of the decreased Ga diffusion length on Si surface. Coalescence of these nucleated crystals then results in a high density of defects. Therefore, the growth temperature of 630 °C is the optimized growth temperature.

On the other hand, in order to understand the morphological change in each growth stage, the time evolution growth study was also performed at 630 °C from the deposition duration of 30 minutes to 120 minutes as displayed in Fig. 3. The growth initiated from one particular nucleation site, i.e. mostly on the edge of SiO_2, and then in the following stages to expand to fill the complete hole region to form the nanodisk arrays. As deposition proceeds, these nucleated GaAs crystals incorporate more material and expand both vertically and laterally to fill the patterned holes as can be seen in Figs. 3(b) and 3(c). Up to 120 min, each individual nanodisk has lateral dimensions of ~1 μm and it fully covers the patterned area [Fig. 3(d)]. It is also identified from the SEM

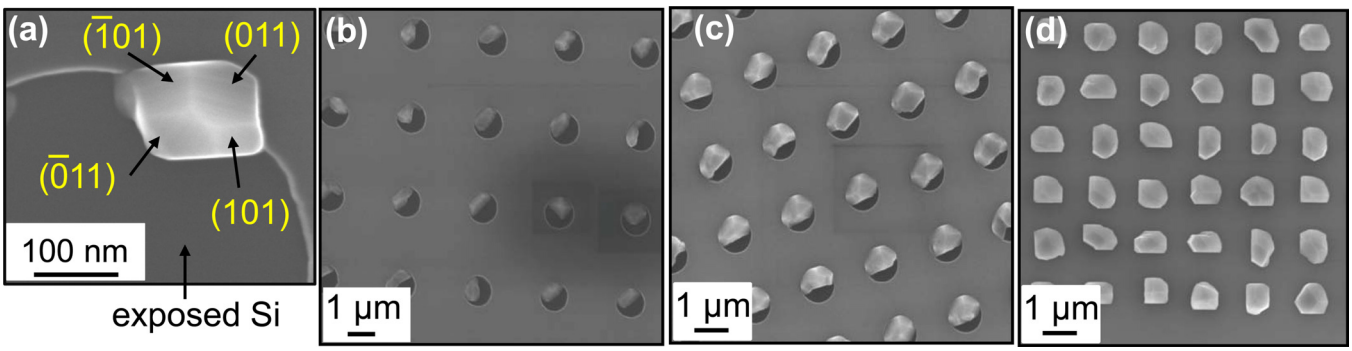

FIG. 3. (Color online) SEM images of time evolution study for SAE grown GaAs nanodisks on Si(100) patterned substrates for (a) 30 min, (b) 60 min, (c) 90 min, and (d) 120 min.

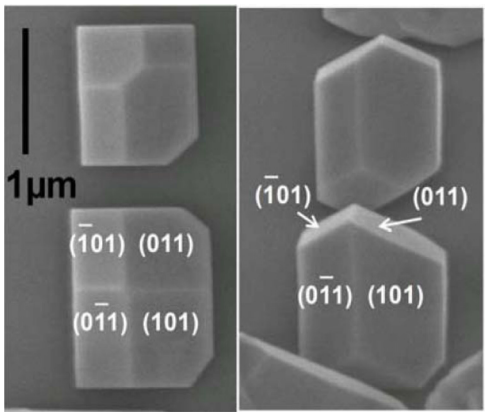

FIG. 4. (Color online) SEM images of two adjacent GaAs nanodisks grown at 630 °C showing {110} side walls and top facets. Left: top view; right: 45° tilted view.

image that these disks have evident facets even at the very beginning, i.e., after 30 min of the growth duration stage. The vertical side walls (four edges of the rectangle from top view) are four {011} planes. The top four facets are other {011} planes. These facets indicate single crystalline nature of the growth and they are associated with the lowest total surface energy in equilibrium.

The growth mechanism of the nanodisk is studied by its morphology at the initial and the final stage of the deposition. When the growth temperature reaches as high as 630 °C, Ga adatoms either desorb on SiO_2 surface or migrate to the nearby opening of silicon surface. These Ga adatoms are then incorporated with arsenic and nucleate in the Volmer–Weber growth mode.[17] Due to the large diffusion length of Ga at this temperature, these nucleations occur at the edges of the circular openings, where Ga atoms migrate to and then stop at the boundary. In addition, it can be clearly seen that the same set of {011} facets present not only in these nucleated crystals at the beginning stage but also in the final stage of the growth as displayed in Fig. 4, which is the magnified view of Fig. 3(d). Such facets formation on the top surface as well as the sidewall indicates the minimization of the total surface energy by strain relaxation in the very beginning stage. Following the idea, as the deposition proceeds, the deposited GaAs crystals retain the strain relaxed nature but expand their size vertically and laterally to form the nanodisks.

GaAs nanodisks grown at 630 °C were further investigated by high resolution XTEM. Figure 5(a) exhibits the relative location of GaAs-Si-SiO_2 interfaces, whereas Fig. 5(b) shows the GaAs laterally overgrown on top of SiO_2 with very few stacking faults and superior crystal quality in this region. The good crystal quality in the overgrown region is possibly due to the complete strain relaxation in the GaAs epilayers within the patterned hole region, so that the

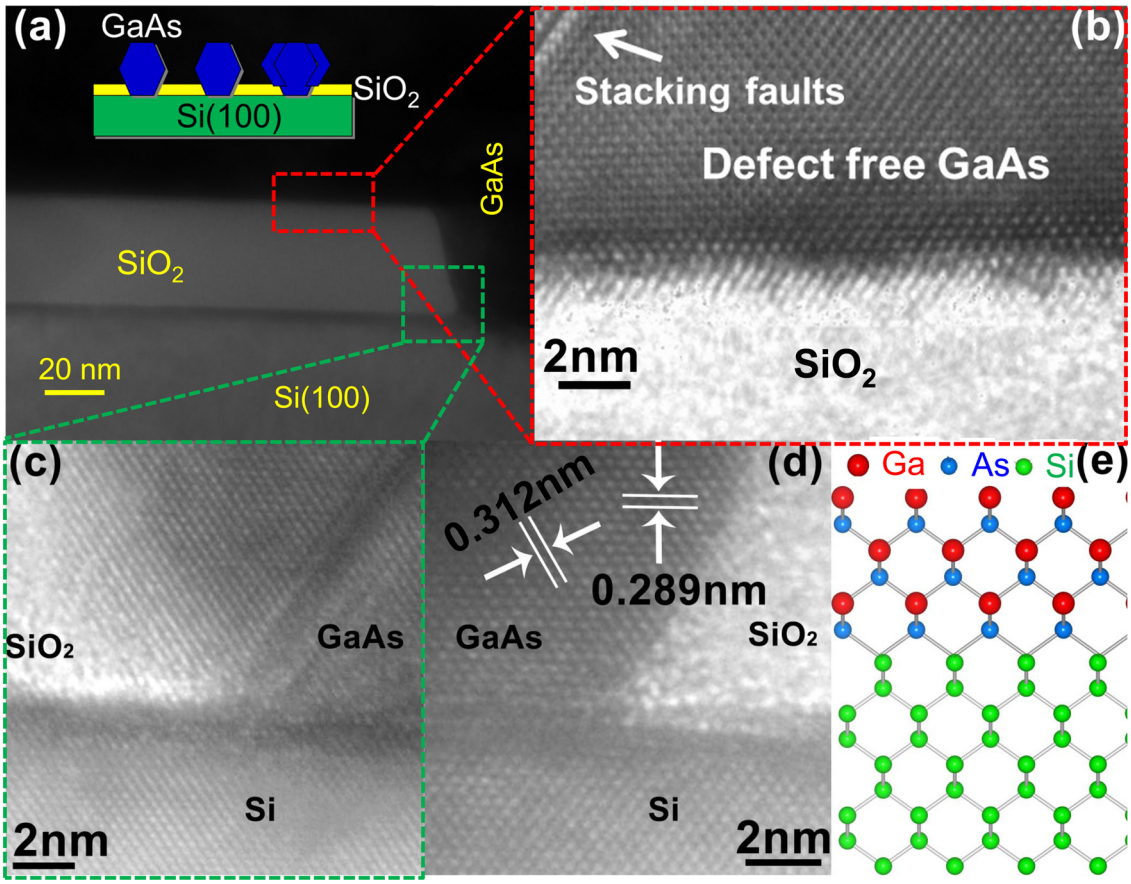

FIG. 5. (Color online) XTEM images of (a) GaAs/Si interface; (b) GaAs laterally overgrown on top of SiO_2 showing very few stacking faults (c) left edge, (d) right edge of GaAs/SiO_2 interface showing defect free nature beyond the edge (defects are constrained only ~2 nm at GaAs/Si interface), and (e) GaAs-Si covalent bond diagram.

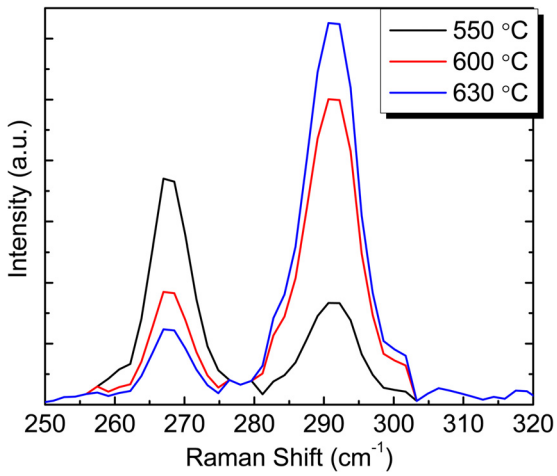

FIG. 6. (Color online) Micro-Raman spectra for GaAs nanodisks grown at different growth temperatures showing the trend of increasing LO/TO intensity ratios with the increasing temperature.

extended growth on the SiO_2 can retain the almost defect-free nature. Furthermore, Fig. 5(c) the left edge and (d) the right edge of GaAs/SiO_2 interface also show threading dislocation and stacking fault free nature beyond the edges. With no observed rotational twin defects and threading dislocations, the good quality of the material corroborates the efficacy of SAE scheme we applied. Although some low-density stacking faults are observed as shown in Fig. 5(c), they are mostly constrained at the edge of the patterned hole. These stacking faults occur when the nucleated GaAs crystal expands to reach the SiO_2 mask as they are possibly one way to release the strain energy. The reduced defect density and the constrained surface misfit dislocations within ~2 nm from the GaAs/Si heterointerface are achieved by nanoscale patterning and lateral overgrowth on top of the SiO_2 mask, these GaAs nanodisk arrays may have a potential for optoelectronic device applications.

Moreover, we employed micro-Raman spectroscopy as a means to nondestructively characterize the GaAs nanodisks crystallinity change and the strain relaxation conditions as the growth temperature varies from 550 °C to 630 °C as shown in Fig. 6. Previous investigations[18,19] have shown the Raman signals from highly perfect single-crystal GaAs consists primarily of the contributions from the longitudinal optical (LO) phonon mode at 292 cm^{-1}. On the other hand, the addition of defects into the structure results in the contributions from the otherwise transverse optical (TO) phonon mode at 268 cm^{-1}. Therefore, the ratio of LO to TO relative intensities in the Raman spectra could be used as the qualitative assessment to understand the crystalline quality of the GaAs nanodisks. Figure 6 exhibits the comparison of the Raman spectra obtained from GaAs nanodisks at different growth temperatures. The remarkable increase of LO mode intensities was observed as the growth increases from 550 °C to 630 °C, indicating the single-crystal dominant structure is formed as the process goes toward the complete SAE. At 630 °C, we observed the largest LO/TO ratio compared to the other two growth temperatures suggesting the much fewer the defects and grain boundaries are incorporated into the epitaxially grown structure. However, there are no peak shifts in the LO and TO modes corroborating the complete strain relaxation in the structures grown at these three growth temperatures due to the merit of the SAE.

Figure 7(a) shows the temperature dependent μ-PL spectra for GaAs nanodisks grown at 630 °C within the hole arrays. We observed the strong direct band-to-band as well as the relatively inhibited defect-induced optical transitions in the temperature range from 77 K to 300 K. As expected, the *PL peaks redshift* and broaden with *increasing temperature* corroborating the luminescence mainly from the direct band-to-band transition. We can hereby attribute the excellent optical property to the tremendously reduced defects and stacking faults at the GaAs/Si interface. Moreover, the contributions from catalyst-free growth mechanism along with the initial low temperature grown GaAs layer effectively suppress the formation of midgap trap centers and unintentional doping from the Si substrate.

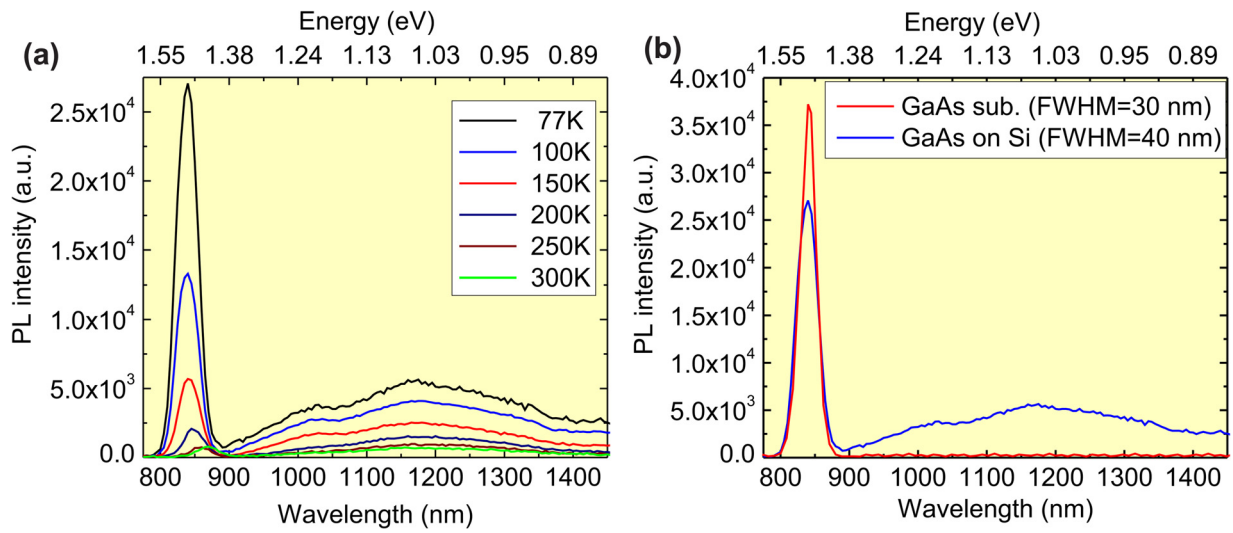

FIG. 7. (Color online) (a) Temperature dependent PL spectra for GaAs nanodisks grown on a patterned Si substrate. (b) PL spectra at 77 K for 1 μm GaAs thin film grown on an intrinsic GaAs wafer vs GaAs nanodisks on Si.

In order to evaluate the quality of our grown nanostructures, we also grew a reference sample with 1 μm GaAs thin film grown on top of intrinsic GaAs wafer at the same growth condition. The 77 K PL measurement was also performed for this reference sample to serve as the comparison set along with our GaAs nanodisks on Si. Compared to the case of GaAs nanodisks-on-Si, GaAs-on-GaAs exhibits slightly stronger PL emission corresponding to direct band-to-band transition and much weaker midgap transitions in the long wavelength regime as displayed in Fig. 7(b). The peak emission intensity of band-to-band recombination for GaAs-on-GaAs is only 1.5 times higher than GaAs nanodisks-on-Si meaning the GaAs nanostructures offer reasonably good quality. In addition, the full width at half maximum of the band-to-band PL emission between these two cases is literally comparable (30 vs 40 nm). In spite of the midgap trap center induced transition possibly due to the defects at the GaAs/Si interface in long wavelength regime, we could still claim the optical property of our GaAs nanodisks grown on patterned are still decent.

IV. SUMMARY AND CONCLUSIONS

We demonstrate the SAE growth of high-quality GaAs nanodisks on patterned Si(100) substrate. SEM and XTEM reveal excellent material quality, which is attributed to relaxation of strain energy by forming facets and the lateral overgrowth scheme. The reduced defect density and the very constrained surface misfit dislocations (only $\sim$2 nm at GaAs/Si interface) are achieved. The strain relaxation and the change in crystallinity from polycrystal-dominant to single crystal-dominant structure with the increasing growth temperature are verified by the micro-Raman spectroscopy. In addition, the excellent material quality contributes to excellent optical properties observed by μ-PL from 77 K to room temperature with luminescence mainly from direct band-to-band transition.

ACKNOWLEDGMENTS

This work was financially supported by the King Abdulaziz City for Science and Technology (KACST), Saudi Arabia, under contract number 20092383 and California Center of Excellence on Green Technology.

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