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# Nanoscale Growth of GaAs on Patterned Si(111) Substrates by Molecular Beam Epitaxy

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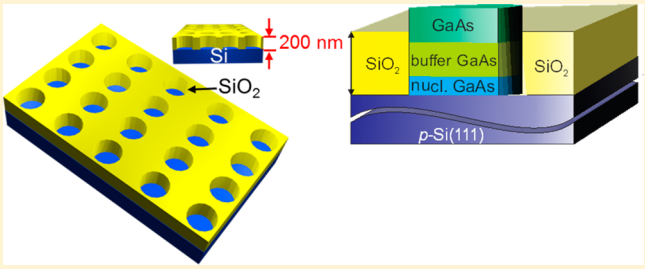
Supporting Information

**ABSTRACT:** High-quality and defect-free GaAs were successfully grown via molecular beam epitaxy on silicon dioxide patterned Si(111) substrates by a two-step growth technique. Compared with the one-step approach, the two-step growth scheme has been found to be a better pathway to obtain a superior-quality GaAs on Si. Taking advantages of low energy for both Si(111) surface and GaAs/Si(111) interface, the two-step grown GaAs of total ~175 nm atop patterned Si(111) substrates exhibits atomically smooth surface morphology, single crystallininty and a remarkably low defect density. A low-temperature GaAs nucleation layer of the two-step growth helps relieve the misfit stress by accommodating the misfit dislocations at the very adjacent GaAs/Si interface. The excellent properties of the two-step grown GaAs were investigated and verified by field-emission scanning electron microscopy, atomic force microscopy, X-ray diffraction, transmission electron microscopy, and Raman spectroscopy. Finally we demonstrated a GaAs on Si solar cell, which could represent an important milestone for future applications in light-emitting diodes, lasers, and photodetectors on Si.




## 1. INTRODUCTION

Since the 1980s, III−V compounds epitaxially grown on Si substrates have attracted a great deal of interest because of the monolithic integration of optoelectronic devices with Si-based microelectronics.[1−3] In fact, successful heteroepitaxial growth will not only provide high carrier mobility and direct bandgap III−V materials but also maintain the advantages of lightweight and low-cost Si substrates with high mechanical strength and excellent thermal management. To date, researchers have extensively focused on the growth of high quality III−V compounds on Si and accomplished the so-called bottom-up integration. However, obtaining high crystal quality III−V compounds, such as GaAs on Si is still challenging because of anti-phase domain (APD) boundary formation as the result of the polar GaAs growth on nonpolar Si system; a high density of threading dislocations generated by 4.1% lattice mismatch along with 62% thermal expansion coefficient mismatch.

To circumvent such intrinsic mismatch problems, several approaches, such as time-consuming and complex thermal cycling process,[4−6] quantum dots dislocation filters,[7] strained layer superlattice (SLS) buffer layers,[8] and micrometer-thick graded buffer layers[9] have been employed for the epitaxial growth. However, these techniques are not cost-effective and would even complicate the growth procedures. Recently, the patterned growth scheme has been demonstrated as an excellent alternative to obtain high quality GaAs and other materials on silicon dioxide ($SiO_2$) patterned Si substrates.[10−13] Most importantly, this growth scheme can effectively mitigate these three major mismatch problems.[14] Instead of misoriented (vicinal) Si substrates, this patterned growth approach using nominal Si substrates could also effectively reduce the probability of forming high-density APD boundaries. Hence, the nominal Si substrates could be chosen as starting material in our work. However, the surface energy for different planes must be carefully considered in order to achieve the high-quality GaAs atop Si. As opposed to Si(100) plane, Si(111) plane has a lower surface energy.[15] In addition, the lower GaAs/Si(111) interface energy would further facilitate Frank-van-der-Merwe (FM) layer-by-layer growth mode. Meanwhile, we can also benefit from the use of $SiO_2$ sidewalls in stopping and hindering the propagation of the threading dislocations. Consequently, a much thinner GaAs epilayer with a substantially reduced number of defects is expected to be grown on patterned Si(111) substrates. In addition to these obvious advantages, the patterned growth technique eliminates

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the need for patterning postgrowth mesas, while the $SiO_2$ sidewalls can automatically serve as a lateral electrical isolation.

Recently, such patterned growth approach for GaAs/Si has been demonstrated by numerous research groups.[14,16−20] A nanopatterned growth approach was used here to obtain continuous and large-scale micrometers-thick GaAs films on Si(001) substrates by metal−organic vapor-phase epitaxy (MOVPE).[21,22] However, the growth process reported here utilized a growth temperature as high as 650 °C and the $\mu$m-thick overgrown GaAs epilayers which are incompatible for the back end of line (BEOL) Si technology and unfavorable for GaAs to Si integration. In particular, a growth temperature more than 600 °C is not suitable for the metallization in Si devices. Also, because of a lower thermal conductivity of GaAs compared to Si, the thick GaAs buffer layer is inappropriate for an efficient thermal management in these devices.

In this paper, we demonstrate such GaAs to Si integration at a growth temperature of 600 °C utilizing the two-step scheme on Si(111) patterned substrates. In doing so, the large misfit stress between GaAs and Si is relieved by misfit dislocations at GaAs/Si interface which are introduced by low-temperature (400−450 °C) grown GaAs nucleation layer in the first step. The nucleation layer was relaxed to a nearly stress free state, and therefore a thick GaAs could be readily grown at a higher temperature (550−600 °C) by homoepitaxy. Furthermore, we demonstrate that the two-step conformal epitaxy could successfully not only generate high-quality and ultrathin GaAs layer atop Si substrates, but also make the GaAs surface facet-free, beneficial for planar optoelectronic devices. Through comprehensive morphological, structural and crystallinity characterizations, we conclude that the two-step growth scheme is a viable approach to achieve ultrathin, atomically smooth, single-crystalline GaAs epilayer grown in the patterned holes. Finally, a *p-i-n* heterojunction was fabricated based on the *i*-GaAs buffer layer capped with a $n^+$-GaAs atop the *p*-Si substrate. Thus, photovoltaic devices were realized to illustrate the utility of such buffer layer.

## 2. EXPERIMENTAL DETAILS

First, a 200-nm-thick thermal $SiO_2$ was grown on Si(111) substrates. Arrays of circular holes with a diameter of 1 $\mu$m were defined by stepper lithography followed by the subsequent inductive coupled plasma reactive ion etching (ICP-RIE) of the top $SiO_2$ layer. Representative scanning electron microscopy (SEM) images of patterned circular holes and the corresponding schematics are shown in Figures 1a and b.

Prior to the epitaxial growth, the patterned substrates were chemically cleaned by the standard RCA process.[23] Next, the substrates were immersed in a 2.5% diluted hydrofluoric acid (HF) for 30 s at room-temperature (RT) to strip the thin oxide layer and some traces of ionic contaminants. The cleaned samples were degassed at 400 °C for 10 min in the buffer tube of our Perkin-Elmer 430 MBE system prior to loading into the growth chamber. Afterward, the thermal treatment was applied at 900 °C for 10 min in the growth chamber to remove residual native oxides, which might have formed during loading, and to make the surface hydrogen-free.[24,25] Subsequently, the growth of high quality GaAs layers on Si was performed under an Arsenic (As) beam equivalent pressure of around $2.7 \times 10^{-4}$ Pa ($2 \times 10^{-6}$ Torr). In order to ascertain a high-quality epilayer through the two-step process, we also grew GaAs atop Si(111) patterned substrates via one-step, i.e. a self-assembled growth approach as the control samples for comparison. Both of one-step and two-step growth schemes were initiated after turning the exposed Si surface inside the patterned circular holes into the As-terminated one. This was done by exposing the patterned substrates under the As overpressure for 5 min.

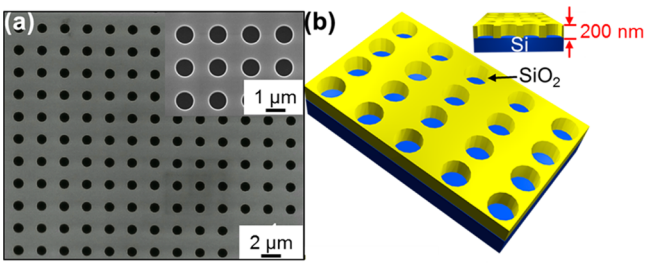


**Figure 1.** (a) SEM images for arrays of patterned holes with 1 $\mu$m diameter formed by stepper lithography, where the dark circular holes are exposed Si surface. (b) Schematics of tilted and cross-section views for patterned Si substrates with a 200 nm thick $SiO_2$ mask.

The surface morphology of as-grown GaAs structures was characterized by SEM (JEOL, JSM-6700F) and atomic force microscopy (AFM, VEECO Nanoscope IIIa Multimode SPM) in the tapping mode. To determine the crystalline quality, the as-grown patterned structures were studied using a high resolution X-ray diffractometer (HRXRD, Bruker D8 Discover) with a monochromatic CuK$\alpha$ ($\lambda$ = 1.5405 Å) radiation source operated at 45 kV and 40 mA. The structural and crystalline quality of GaAs were further investigated by cross-sectional transmission electron microscopy (XTEM, JEOL, JEM-3000F) with the specimens prepared by gallium focused ion beam (Ga-FIB) milling with precoated chromium, gold, and platinum films as protective layers. Furthermore, the micro-Raman spectra on the as-grown patterned structures were obtained at RT by using a Raman spectrometer (Renishaw Raman microscope) with a 532 nm excitation laser.

## 3. RESULTS AND ANALYSIS

Prior to discussing the experimental results, at first the models of both one- and two-step growth initiation and continuation processes on Si(111) substrate are schematically shown in Figure 2. For the one-step growth, GaAs is grown directly at a substrate temperature as high as 630 °C with a V/III ratio of 10. The faceted GaAs was grown for 1 $\mu$m in thickness at the nominal growth rate of 1 Å/s. The morphological evolution of such GaAs nanostructures over time is described in the Supporting Information (Figure S1). In this growth method, both nucleation and growth occur at a high temperature so that the nuclei can easily have different orientations with respect to the substrates. Accordingly, the misoriented nuclei are easily formed and the nucleation occurs predominantly at heterogeneous sites as schematically illustrated in Figure 2a(i). Because of the high substrate temperature in this growth process, both the nucleation rate and the density of nuclei on the substrate surface remain low. Furthermore, since the free energy barrier for heterogeneous nucleation is also low compared to that of homogeneous nucleation, the growth rate is high and the misoriented nuclei grow and coalesce rapidly to form polycrystalline structures. Consequently, continuation of the growth at this high temperature results in thickening of this polycrystalline layer,[26] which are corroborated with our experimental data described later.

In contrast, for the two-step growth, a 25-nm-thin GaAs nucleation layer at 400 °C was initiated with a V/III ratio of 25 and a slow growth rate at 0.25 Å/s. Then without any interruption, a subsequent thicker GaAs layer of 150 nm was grown at 600 °C with a V/III ratio as high as 100 and a growth rate of 1 Å/s. For each temperature ramping stage, a low ramp rate at around 0.1 °C/s was used to mitigate the influence of the thermal expansion coefficient mismatch issue. In this


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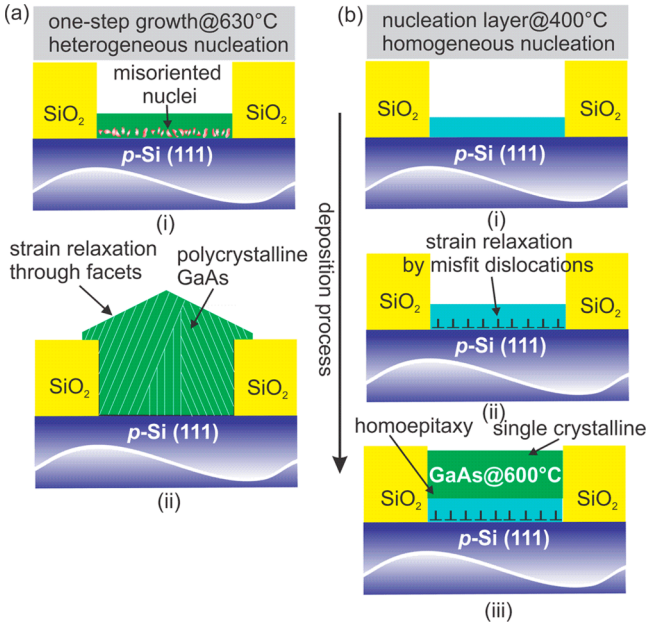


**Figure 2.** Schematic illustrations of two different growth schemes at different stages. (a) One-step growth model: (i) growth initialization at 630 °C through the formation of misoriented nuclei without misfit dislocations, (ii) polycrystallinity of GaAs and the facet formation as the growth continues. (b) Two-step growth model: (i) deposition of nucleation layer at 400 °C, (ii) introduction of misfit stress and its relaxation through misfit dislocation, and (iii) deposition of high-quality GaAs at 600 °C.

process, the low-temperature GaAs nucleation layer regrows epitaxially in the so-called solid phase epitaxial (SPE) growth mode during the heating process before the subsequent high temperature (600 °C) step. Since the low-temperature (400 °C) grown nucleation layer consists of mostly homogeneous small nuclei in parallel epitaxy with the substrate, this layer is not under misfit stress (Figure 2b(i)). Hence the film resulting from coalescence of growing nuclei is essentially single-crystalline with only few misoriented grains embedded in it.[27] However, as the temperature increases, the misfit stress is induced at the regrown GaAs/Si interface because of the inherent thermal expansion coefficients mismatch induced lattice constants change. To accommodate the misfit stress, the misfit dislocations are formed at the interface as schematically shown in Figure 2b(ii). At the higher growth temperature step, the lattice constant of the nucleation layer recovers to the bulk lattice constant of GaAs. Thus, a thick subsequent layer can be readily grown since growth mode is turned into homoepitaxy and the mode changes from a 3D to a 2D layer-by-layer mode.

Now the experimental results of both growth methods will be described in details. For the one-step growth scheme, hexagonally faceted GaAs epitaxial films were obtained as shown in Figures 3a and b. The results achieved by this growth process are similar to what have been reported elsewhere[10,28] The selectivity of this self-assembled growth scheme is achieved due to the long migration length of Ga adatoms and their remarkable desorption from the $SiO_2$ mask at this high temperature. These Ga adatoms are rapidly incorporated with As, yielding self-assembled islands on the nucleation layer through the Volmer–Weber (VW) growth mode. The faceted nature of the as-grown crystals, showing the lower surface energy planes, lead to three (011) facets on the sidewalls and the other three (011) for the top facets. The stress is laterally

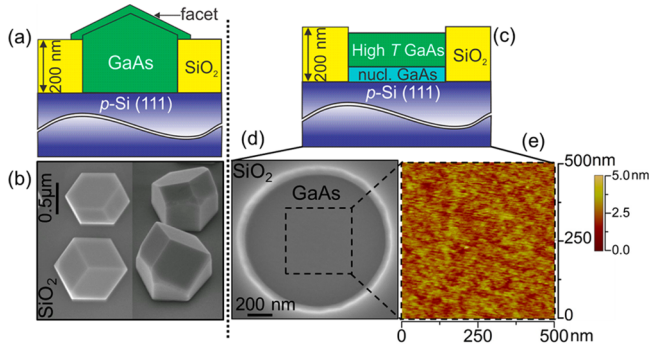


**Figure 3.** Schematic cross-sectional views of GaAs via (a) one-step and (c) two-step growth scheme. (b) SEM plan-view and 45° tilt-view images for self-assembled GaAs crystals. (d) SEM plan-view image of GaAs within the patterned circular hole. (e) Corresponding 0.5 $\mu$m × 0.5 $\mu$m AFM image for the selected region in (d) showing the ultrasmooth surface morphology of GaAs.

relaxed through the formation of top facets and sidewalls in this structure. Moreover, we observed the lateral overgrowth of the crystals protruding from the patterned holes toward the $SiO_2$ masks, indicating the minimization of total surface energy in the lateral direction by forming energetically favorable surfaces. However, the strain relaxation in the self-assembled growth through this faceting formation manner is not preferred for realistic planar optoelectronic device applications due to the uneven surfaces and faceted textures. Alternatively, the two-step based layer-by-layer growth is desirable for planar optoelectronics technology.

For the two-step growth scheme, the grown structures as schematically illustrated in Figure 3c were subjected to different characterization studies. Figures 3d and e show the close-up SEM plan-view and the AFM image, respectively for such as-grown GaAs. The film exhibits atomically smooth surface morphology and high selectivity on the patterned substrates. The ultrasmooth GaAs possess a peak-to-peak variation of only 2 nm and root-mean-square (RMS) roughness value of 0.4 nm which are lower than the lowest-ever reported values obtained on nominal Si substrates.[29,30]

The crystalline quality was further characterized by XRD omega–2 theta and omega rocking curve scans as displayed in Figure 4. The patterned grown GaAs through the two-step growth exhibits superior single-crystalline characteristic as illustrated in Figure 4a. The rocking curve full-width at half-maximum (fwhm) for the GaAs(111) plane is as low as 205 arcsec. The superior surface morphology and crystalline quality from the two-step grown samples could be attributed to the effective reduction of threading dislocations and APD boundaries. These were achieved by the strain relaxation from the low-temperature to high-temperature transition and the constrained finite size growth from the patterned substrates. Since the nucleation for the two-step growth was carried out at a low temperature, the nucleation was predominantly homogeneous and these nuclei were with a parallel orientation with respect to the substrates. In this case, the lateral growth rate of the homogeneously formed nuclei is much faster than those heterogeneously formed nuclei misoriented with respect to the substrates.[31] Moreover, this parallel epitaxy may even consume the nonparallel clusters by grain boundary migration.[31] Consequently, the density of the nuclei is so high that they only need to grow by a very small amount before they coalesce. Meanwhile, the chance for any inclusion of


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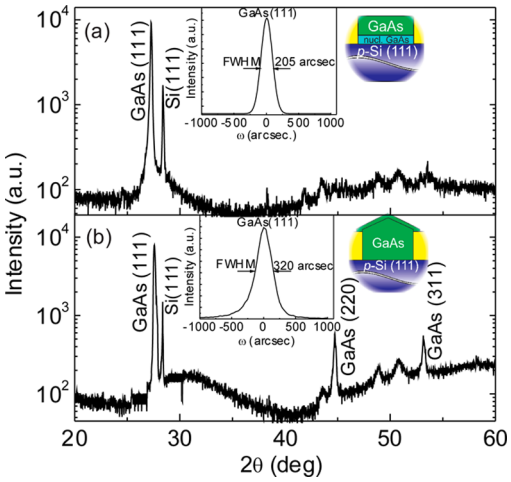


**Figure 4.** (a) XRD omega−2 theta scan for structures grown by (a) two-step growth scheme showing nearly single-crystallinity and (b) one-step (self-assembled) growth scheme showing poly crystallinity with the presence of GaAs(220) and (311). Two insets show their corresponding rocking curves of GaAs(111) peaks.

misoriented nuclei which could lead to polycrystalline nature is further reduced. Accordingly, the high nucleation rate and the high-density of nuclei contribute to their quick coalescence to form a continuous thin and single-crystalline layer on the substrates. On the other hand, the one-step grown GaAs structures exhibit polycrystalline nature, which is confirmed from many diffraction peaks from (111), (220), and (311) crystal planes as shown in Figure 4b. In addition, a larger fwhm value of 320 arcsec is also seen. This worse crystalline quality obtained from the one-step growth could be ascribed to a larger amount of defect formation along both $SiO_2$ sidewalls and GaAs/Si interfaces caused by the higher growth rate during this single step growth.

Moreover, such two-step grown GaAs possesses a much thinner epilayer with similar or comparable crystalline quality compared with former results which used $\mu$m-thick SLS or complex graded buffer layers plus lots of time-consuming thermal cyclic annealing processes.[4−6,8,9] The crystalline quality is further evidenced by the average crystallite size, which is calculated from the fwhm of the XRD omega-scan peaks based on Debye−Scherrer formula[32]

$$D = \frac{1.2\lambda}{\mathrm{FWHM}(2\theta) \times \cos\theta}$$

where fwhm is for the most prominent XRD $2\theta$ peak, and $D$ is the crystallite size. In our case, the dominating peak is GaAs(111) at around 27.3°. Thus the crystallite sizes obtained are 140 and 122 nm for the two-step and one-step samples, respectively. For this crystallite size approximation, we exclude the peak broadening contributed from the instrument and the strain from the epilayers because of the appropriate use of the optics in the measurements and the strain relaxation in the epilayers.

The local structural quality of the two-step grown GaAs was further characterized by TEM. Figures 5a and b show the high angle annular dark field (HAADF) and the bright field (BF) XTEM images, respectively. It is observed that the surface misfits are mainly confined within ~3 nm from the GaAs/Si heterointerface and no obvious threading dislocations are seen as compared with those of the one-step growth.[33,34] These

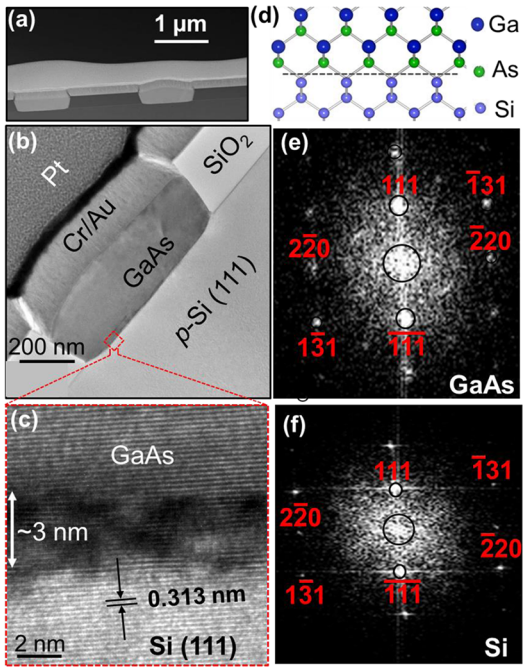


**Figure 5.** (a) HAADF XTEM image of GaAs/Si(111) grown by the two-step growth scheme. (b) close-up view of BF XTEM image of GaAs/Si(111), demonstrating the confinement of the defects at the GaAs/Si interface and threading-dislocation-free GaAs beyond the interfacing layer. (c) HRTEM image of GaAs/Si(111), indicating that the misfit dislocations are confined within a few nm region near the GaAs/Si interface. (d) GaAs/Si covalent bond diagram. (e) and (f) SAED patterns taken for GaAs epilayer and Si, respectively, indicating the GaAs layers were epitaxially grown on Si(111) substrates following the same single-crystalline orientation.

misfits occurred when GaAs crystals nucleated on Si(111) during the first lowtemperature growth step as a result of possible excess Ga adatoms at the beginning of the growth. Figure 5c shows a high resolution TEM (HRTEM) image of the selected region at the GaAs/Si interface exhibiting threading-dislocation-free characteristics. Moreover, based on the etch pit density (EPD) study on the two-step grown GaAs epilayer, the defect pit density is measured to be $\sim 7 \times 10^5$ cm$^{-2}$ obtained by counting the etch pits after the sample was immersed in a molten KOH at 350 °C for 30 s. Selected area electron diffraction (SAED) patterns for such two-step grown GaAs epilayer and substrate are also shown in Figures 5e and f, respectively, further affirming the high quality of the GaAs epilayer on Si. Both of the SAED patterns in the $[11\bar{2}]$ zone axis exhibit single-crystalline characteristics, indicating that single crystalline GaAs on Si(111) substrate. Furthermore, the diffraction spots shown in Figure 5e with the Miller indices indicate that the layer is twin- and dislocation-free. Hence, from the above analyses, we may conclude that the structural quality of our GaAs grown through two-step growth scheme is better than those reported, where nominally the high density of rotational twin defects and threading dislocations usually occurred.[6,15] As to the further characterization of such as-grown GaAs, the Supporting Information (Figure S2) can be referred.

The next is to demonstrate the utility of such two-step grown reliable buffer layer for subsequent multilayer growth. For this purpose, a 150-nm-thick GaAs layer was grown at 580 °C on top of a buffer layer. The schematic cross-sectional view of such


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structure is shown in Figure 6a. Followed by an in situ post growth annealing at 680 °C under As overpressure, the film

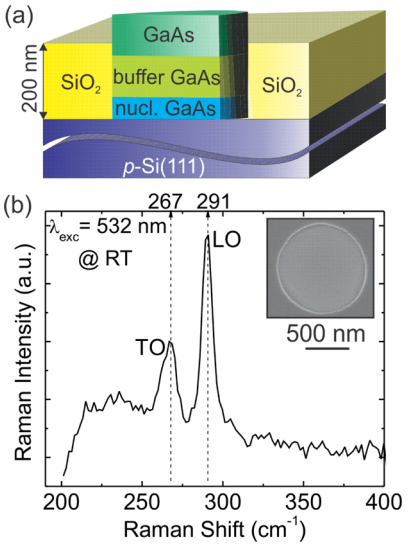


**Figure 6.** (a) Schematic cross-sectional view for a structure consisting of a 150-nm GaAs on top of a high-quality GaAs buffer layer. (b) Micro-Raman spectrum for the as-grown structure at RT. The inset shows an SEM image of the as-grown structure.

properties were investigated by both XRD and micro-Raman spectroscopy. The structure still exhibits single crystallinity confirmed by the XRD pattern which is same as Figure 4a. Figure 6(b) displays the micro-Raman spectrum in which two GaAs Raman signature peaks corresponding to the transverse optical (TO) and longitudinal optical (LO) vibrational bands are located at 267 and 291 $cm^{-1}$, respectively. These strong LO and weak TO bands of GaAs, are slightly red-shifted by 1 $cm^{-1}$ compared to those of bulk GaAs indicating that there are a few defects generated within the GaAs films during the growth process.[35] In spite of being comparable or even better than some of the previous reported results,[35−37] the LO-band fwhm for such as-grown GaAs to be ∼5.8 $cm^{-1}$ is higher than the bulk GaAs which could be attributed to disorder-induced strain relaxation, perhaps arising from point defects formed during the growth.[35]

A prototype *p-i-n* solar cell structure was fabricated using the two-step grown GaAs buffer layer array as schematically illustrated in Figure 7a. The structure, shown in Figure 2b, was modified by adding a 50 nm $n^+$-type heavily doped (2 × $10^{18}$ $cm^3$) GaAs on top of the undoped GaAs buffer layer. Si was used for *n*-doping. The top contact was realized by depositing an indium-tin-oxide (ITO) layer on $n^+$ GaAs, whereas indium was used for the bottom contact. The current density−voltage ($J$−$V$) characteristic of the solar cell is shown in Figure 7(b). In dark, the device exhibits a good rectification characteristic with a current ratio greater than $10^2$ measured at ±1 V bias. The fitted $J$−$V$ curve gives the ideality factor ($\eta$) to be 1.6 at RT. Such low ideality factor could be attributed to high minority carrier recombination at the interface of GaAs and *p*-Si substrate as well as a large series resistance of the top contact. The photovoltaic behavior under solar simulator of one sun AM 1.5G illumination shows $J_{sc}$ = 18.4 mA/$cm^2$ and $V_{oc}$ = 0.18 V. The calculated energy conversion efficiency (ECE) and fill factor (FF) are 0.9% and 28%, respectively. The ECE of this GaAs/Si *p-i-n* based device is comparable or better than the reported values for nanostructured solar cells.[38,39] We attribute this fairly good performance to the high quality buffer layer, which has a very low surface misfit and carrier-trapping threading dislocations. The low FF resulting from a high ideality factor and the low $V_{oc}$ could also be due to the presence of a high density of GaAs surface states adjacent to $SiO_2$ sidewalls and less efficient hole transport across the GaAs/Si heterointerface. It is expected that through proper passivation and improved contact design,[40] the energy conversion efficiency may improve significantly.

## 4. CONCLUSION

We have successfully grown high structural and crystalline quality GaAs on patterned Si(111) substrates through our two-step growth scheme. Utilizing the finite size growth and lower surface energy of Si(111), we have obtained high quality GaAs atop Si with ultrathin (∼175 nm) and ultrasmooth epilayers. The defect-free GaAs epilayer is a potential candidate substrate for planar optoelectronic devices, which shows a pathway to create III−V on Si for many different applications. The fabricated basic *p-i-n* solar cell shows fairly good ECE and FF, and hence can be viewed as an important step toward the broad applications of the III−V compounds to Si integration.

## ■ ASSOCIATED CONTENT

### Supporting Information

Time evolution study of one-step grown GaAs and photoluminescent spectra of two-step grown GaAs are reported here. This information is available free of charge via the Internet at http://pubs.acs.org/.

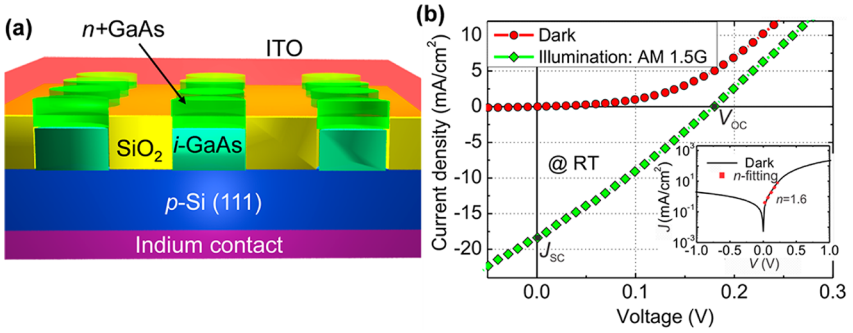


**Figure 7.** (a) Schematic cross-sectional view of the fabricated *p-i-n* solar cell (b) $J$−$V$ characteristics of the device under dark and illumination of one sun AM1.5G; the semilogarithmic plot of dark $J$−$V$ is shown as inset.


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### Notes

The authors declare no competing financial interest.

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# Nanoscale growth of GaAs on patterned Si(111) substrates by molecular beam epitaxy

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## Supporting information

Figure S1 displays SEM images showing a time evolution study for the growth of GaAs on Si(111). In fact, at a growth temperature of 630°C, the evolution of the morphology as a function of deposition time for (a) 30, (b) 60, (c) 90, and (d) 120 min has been presented here. As can be seen, the growth initiates from one particular nucleation site, i.e. mostly on the edge of $SiO_2$ and then expand to fill the complete hole region to form the nanopillars. As deposition proceeds, these nucleated GaAs crystals incorporate more material and expand both vertically and laterally to fill the patterned holes. Each individual nanopillar, as shown in Fig. 1(d), has lateral dimensions of ~1 μm as it fully covers the patterned area. It is also identified from the SEM image that these pillars have evident facets.

Considering further, Ga adatoms either desorb on $SiO_2$ surface or migrate to the nearby opening of silicon surface during the growth. These Ga adatoms are then incorporated with As and nucleate in the Volmer-Weber (VW) growth mode. Due to the large diffusion length of Ga at this temperature, this nucleation occurs at the edges of the circular openings, where Ga atoms migrate to and then stop at the boundary.

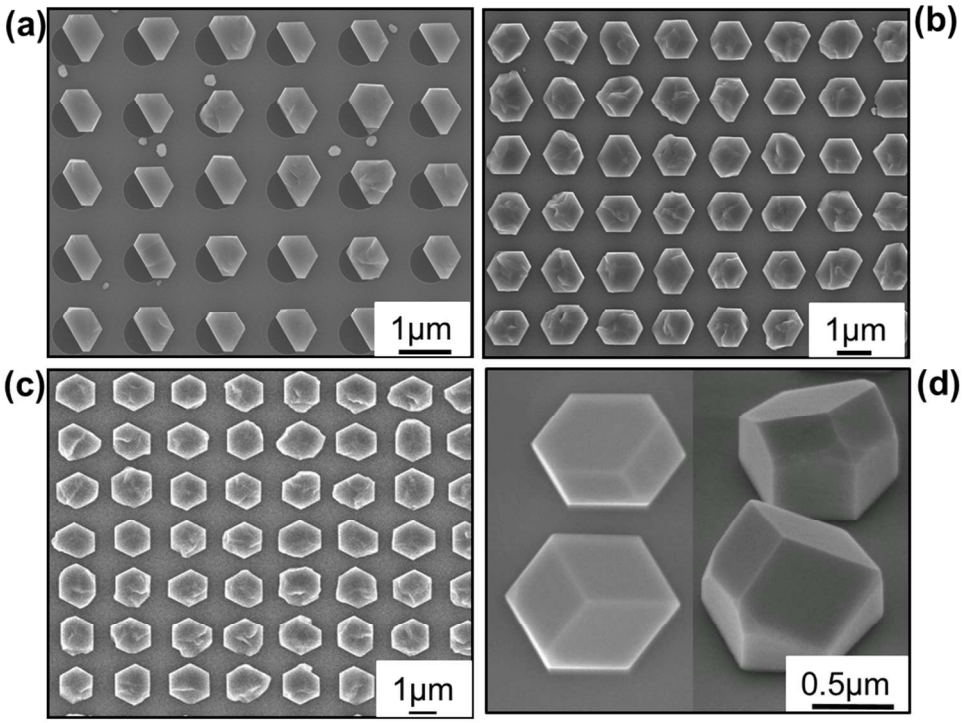


**Figure S1** Time evolution study of GaAs nanopillars grown on Si(111)

Figure S2 shows the temperature dependent photoluminescence (PL) spectra for GaAs grown by 2-step growth scheme within the circular patterned holes. We observed the strong direct band-to-band as well as the relatively inhibited defect-induced optical transitions in the temperature range from 77K to 300K. As expected, the PL peaks redshift and broaden with increasing temperature corroborating the luminescence mainly from the interband transition. In contrast to previously reported results[1-5], our temperature dependent PL spectra have demonstrated the better optical property obtained through our reliable growth scheme.

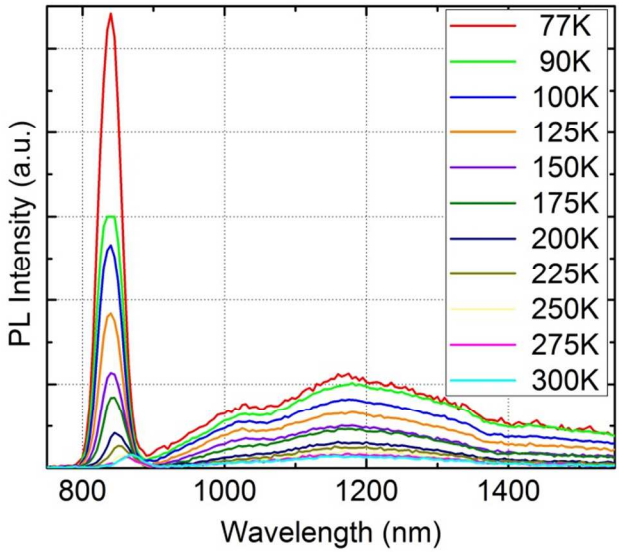


**Figure S2** Temperature-dependent PL spectra of two-step grown GaAs grown on Si (111) in the temperature range 77K - 300K.

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