4-1.5 Ideal Reconstruction

**Ideal D-to-C Conversion**

\[ y[n] \xrightarrow{\text{discrete}} \text{Ideal D-to-C Converter} \xrightarrow{\text{continuous time}} y(t) \]

\[ f_s = \frac{1}{T_s} \]

\[ y(nT_s) = y[n] \]
Real D to C converter

(DAC → Digital to Analog Converter)

$y[n]$

Interpolation

Zero order hold reconstruction

First order reconstruction (linear interpolation)

A DAC connects the dots via interpolation
A DAC "catches on" to the principal alias
\[ \hat{\omega}_1 = \hat{\omega}_0 + 2\pi \]

unique frequencies

\[ \hat{\omega} \]

principal alias

radious/sample

cycle/sample

unique frequencies

\[ \hat{f} = \frac{\hat{\omega}}{2\pi} \]

\[ \hat{f} = \frac{f}{f_s} \]

\[ f = \hat{f} f_s \]

\[ \hat{f}_0 = f_0 \]

\[ f_1 = \hat{f}_0 + 1 \]

\[ \frac{f_1}{f_s} = \frac{f_0}{f_s} + 1 \Rightarrow f_1 = f_0 + f_s \]
$\text{DAC will latch on to this frequency}$
$f_{\text{max}} < \frac{f_s}{2}$

Ideal DAC will reconstruct the signal exactly.

Original signal will not be recovered. DAC will fold these frequencies to the range $\left[-\frac{f_s}{2}, \frac{f_s}{2}\right]$. 
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The diagram illustrates the concept of aliasing and how it affects signal processing. The text "DAC will fold" indicates that the DAC (Digital Analog Converter) will fold at a certain frequency. The inequality \( f_{\text{max}} > \frac{f_s}{2} \) shows the condition for avoiding aliasing, where \( f_{\text{max}} \) is the maximum frequency of the signal and \( f_s \) is the sampling frequency. The arrows and annotations help in visualizing the folding and aliasing effects in the frequency domain.
Example

$4 \cos(100\pi t)$ → $\text{Ideal D to C converter}$ → $v_{\text{out}}(t)$?

$f_s = 150 \text{ Hz}$

$\hat{f}$, $\hat{\omega}$

$\frac{f_s}{2}$, $\frac{f_s}{2}$

No aliasing

$v_{\text{out}}(t) = 4 \cos(100\pi t)$
Example

\[ V_{out}(t) = 4 \cos(40 \pi t) \]

**Distortion!**