9.6 Programmable Logic Devices (PLD)

PLA (Programmable Logic Arrays)

Realizes selected (programmed) product terms.

Can realize m functions of n variables.

Same basic function as a ROM, but implements m output lines sum of product expressions (instead of sum of minterms).

ROM directly implements the truth table (sum of minterms).

\[ \text{PLA} \longrightarrow \]

\[ \text{AND Array} \]

\[ \text{OR Array} \]

Input Lines

\[ n \]
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Example:

\[ f_1 = a'bd + abd + ab'c' + b'c \]
\[ f_2 = c + a'bd \]
\[ f_3 = bc + ab'c' + abd \]

<table>
<thead>
<tr>
<th></th>
<th>a</th>
<th>b</th>
<th>c</th>
<th>d</th>
<th>f_1</th>
<th>f_2</th>
<th>f_3</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>a'd</td>
<td>0</td>
<td>1</td>
<td>-</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>abd</td>
<td>1</td>
<td>1</td>
<td>-</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>ab'c'</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>-</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>b'c</td>
<td>-</td>
<td>0</td>
<td>1</td>
<td>-</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>c</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>-</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>bc</td>
<td>-</td>
<td>1</td>
<td>1</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Inputs: unlike a ROM more than one word lines can be equal to 1
When the number of inputs is small a PROM may be more economical than a PLA.

To realize eight functions of 24 variables would require a PROM of $2^{24} \approx 16$ Million 8 bit words!

The outputs of several PLAs can be ORed together to handle bigger functions
Programmable Array Logic (PAL)

Programmable Node

Programmable Nodes

X
Y
C_in

Programmed
Unprogrammed

Unprogrammed PAL
\[ \text{conventional symbol} \]

\[ \text{array logic symbol} \]
\[ \text{Sum} = XYC_{in} + XYC_{in}' + XYC_{in} + XYC_{in} \]
\[ C_{out} = XC_{in} + YC_{in} + XY \]

Unlike the PLA, the AND terms cannot be shared among two or more gates. The number of AND terms per OR gate is fixed and limited.