9.2 Multiplexers (MUX)

Data Inputs

\[ I_o \quad I_1 \]

\[ Z \]

2-to-1 MUX

Control Input

\[ A = 0 \]

\[ I_o \]

\[ I_1 \]

\[ Z = A' I_o + A I_1 \]

\[ 2^n \] data lines

\[ 2^n \] to-1 MUX

\[ 2^n \] to-1 MUX

\[ n \] control inputs
\[ Z = \sum_{k=0}^{2^n-1} m_k I_k \]

\[ Z = A'B'I_o + A'BI_1 + AB'I_2 + ABI_3 \]

\[ I_0, I_1, I_2, I_3 \]

\[ 2^3 = 4 \]

\[ 2 - 1 \text{ MUX} \]
E = 0
Z = 0 independent of inputs  (MUX disabled)
E = 1  MUX behaves normally  (MUX enabled)

E active high enable
(E = 1 → circuit behaves as a MUX)

E active low enable
(E = 0 → circuit behaves as a MUX)
9.3 Three State Buffers

Three state logic

\[ B = 1 \Rightarrow C = A \]
\[ B = 0 \Rightarrow C = \text{hiZ infinitez} \]

<table>
<thead>
<tr>
<th>BA</th>
<th>C</th>
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<tbody>
<tr>
<td>00</td>
<td>Z</td>
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<tr>
<td>01</td>
<td>Z</td>
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<tr>
<td>10</td>
<td>0</td>
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<tr>
<td>11</td>
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Active low

Active high
Data selection

\[
\begin{array}{cccc}
A & B & C & D \\
\hline
\end{array}
\]

\[
\begin{array}{cccc}
A & Z & D \\
\hline
1 & & & \\
C & & & \\
\end{array}
\]

\[
\begin{array}{cccc}
A & B & S1 & S2 \\
\hline
X & X & X & X & X & X \\
0 & X & 0 & X & 0 \\
1 & X & X & 1 & 1 \\
Z & X & 0 & 1 & Z \\
\end{array}
\]

X (unknown)
4-bit adder with 4 sources

4-bit adder

A
B
C
D

E

Sum

C_out
Bidirectional pins

input

Logic circuit

output

Bi-directional

input pin or output pin

not both at the same time

input

Logic circuit

output

Bi-directional

output signal

input

Logic circuit

output