7.1 Multiple-Level Gate Circuits

Levels of gates: Maximum number of gates connected between a circuit input and the output.

Two level: sum of products, product of sums (SOP) (POS)

$$f = a'c'd + bc'd + bcd' + acd'$$

Comming from Level 1

Flipflops where both $a$ and $a'$ is available.

SOP

AND-OR

Two levels

Five gates

16 gate inputs
\[ f = (b + c + d')(a+b'+d)(a'+b+d')(a'+b'+c) \]

The number of levels in an AND-OR circuit can usually be increased by factoring the SOP expression from which it was derived.

\[ f = a'c'd + bc'd + bcd' + acd' \]

factor

\[ = c'd(a'+b) + cd'(a+b) \]
\[ c'd(a' + b) + cd'(a + b) \]

![Logic Diagram]

Example:

\[ f(a, b, c, d) = \sum m(1, 5, 6, 10, 13, 14) \]

Truth Table

\[ a'c'd + bc'd + bcd' + acd' \]
product of sums

\[ f' = c'd' + ab'c' + cd + a'b'c \]

\[ f = (c + d)(a' + b + c)(c' + d')(a + b + c') \]

Two levels
Five gates
14 gate inputs
Best two level solution
The number of levels in an OR-AND circuit can usually be increased by multiplying out some of the terms in the POS expression from which it was derived.

\[
f = \frac{(c + d)(a' + b + c)(c' + d')(a + b + c')}{(c + d(a' + b))(c' + d'(a + b))}
\]

using \((x + y)(x + z) = x + YZ\)

\[
f = (c + d(a' + b))(c' + d'(a + b))
\]

\[
= (c + a'd + b'd)(c' + ad' + bd')
\]

Three levels
Seven gates
16 gate inputs
8.3 Gate Delays & Timing Diagrams

When the input to a logic gate is changed, the output will not change instantaneously.

[Diagram showing input and output signals with time axis and propagation and delay times marked with \( \varepsilon \) and \( \varepsilon_1 \) to \( \varepsilon_2 \).]

Typical \( \varepsilon \approx 10^{-9} \) s
Timing Diagrams

\[ A \uparrow \quad G_1 \quad G_2 \]

\[ B = 1 \quad C = 0 \]

Assume \( \tau = 20 \text{ ns} \)

held at constant values

\[ A \]

\[ G_1 \]

\[ 0 \quad 20 \quad 40 \quad 60 \quad 80 \quad 100 \quad 120 \quad 140 \]

\[ t(\text{ns}) \]

\[ \leq 40 \text{ ns} \]

\[ \leq 40 \text{ ns} \]

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8.4 Hazards in combinational circuits

Static 1-hazard

Dynamic Hazard

Static-1 Hazard

\[ X + X' = 1 \]
\[ F = AB' + BC \]

Fix \( A = 1 \) & \( C = 1 \)
\[ F = B + B' \]

- Gate delay 10ns
- Not gate delay 2ms
- Others 10ns

- Static-1 Hazard
- 2ns wide
- This glitch might not show up if inertial delay \( > 2\)ns

If inertial delay = 0 then gate is said to have ideal or transport delay

cause of glitch

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If any two adjacent 1's are not covered by the same rectangle, a 1-hazard exists.
Zero hazards

$XX' = 0$
\[ F = (A + c)(A' + D')(B' + c' + D) \]

![Logic Diagram](image)

\[ \begin{array}{c|c|c|c|c|c}
  A & B & C & D & F \\
  \hline
  0 & 0 & 0 & 0 & 0 \\
  0 & 0 & 0 & 1 & 1 \\
  0 & 1 & 0 & 0 & 0 \\
  0 & 1 & 0 & 1 & 0 \\
  1 & 0 & 1 & 0 & 1 \\
  1 & 0 & 1 & 1 & 1 \\
  1 & 1 & 1 & 0 & 1 \\
  1 & 1 & 1 & 1 & 1 \\
\end{array} \]

\[ A = 0, B = 1, D = 0 \& C \text{ changes from 0 to 1} \]
\[ F = (A + c)(A' + D')(B' + c' + D) = C \text{ glitch} \]

See fig. (c) page 226
Eliminate glitch

\[ F = (A + c)(A' + D')(B + c + D')(C + D')(A + B + D)(A' + B' + c) \]